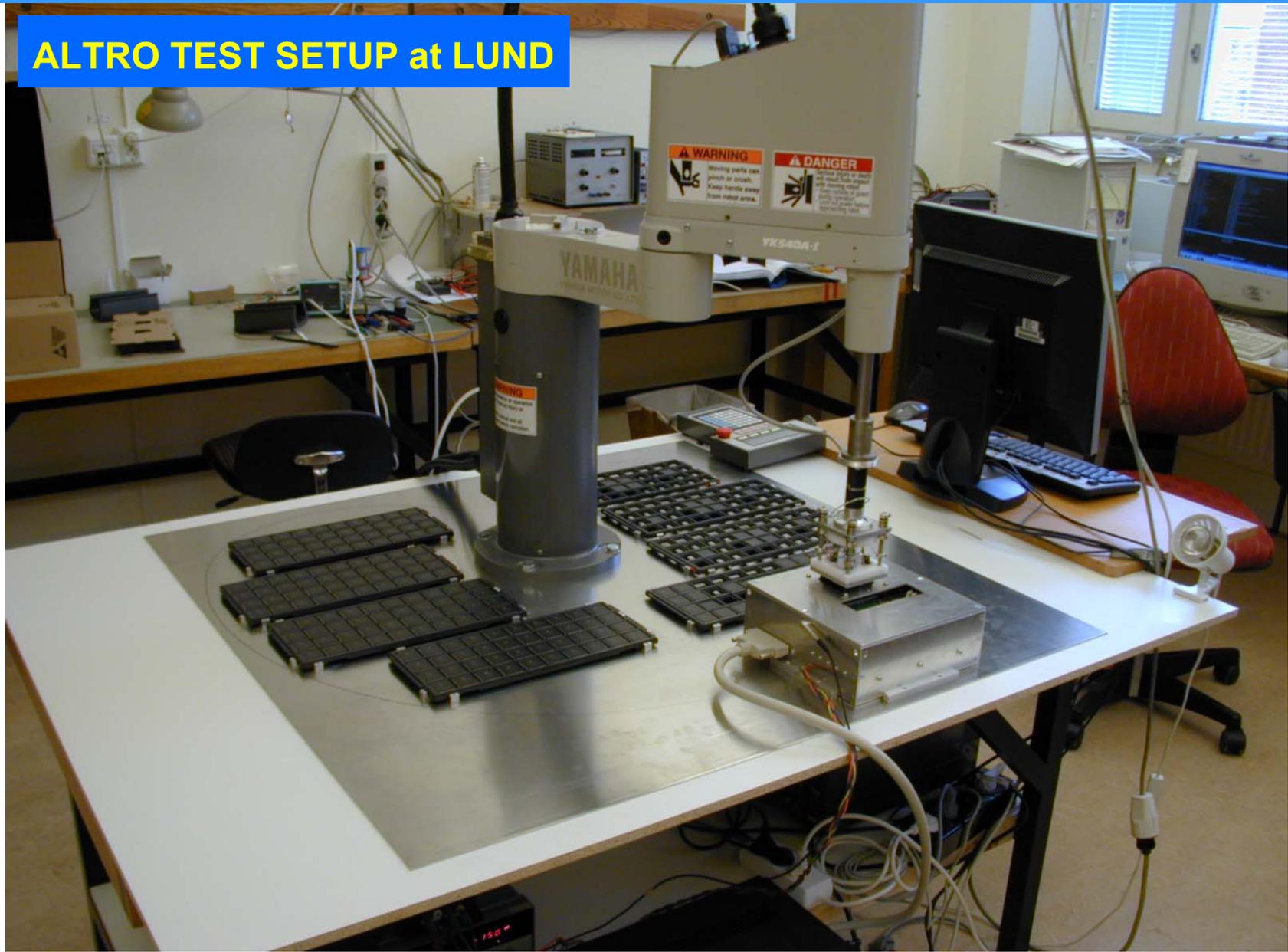


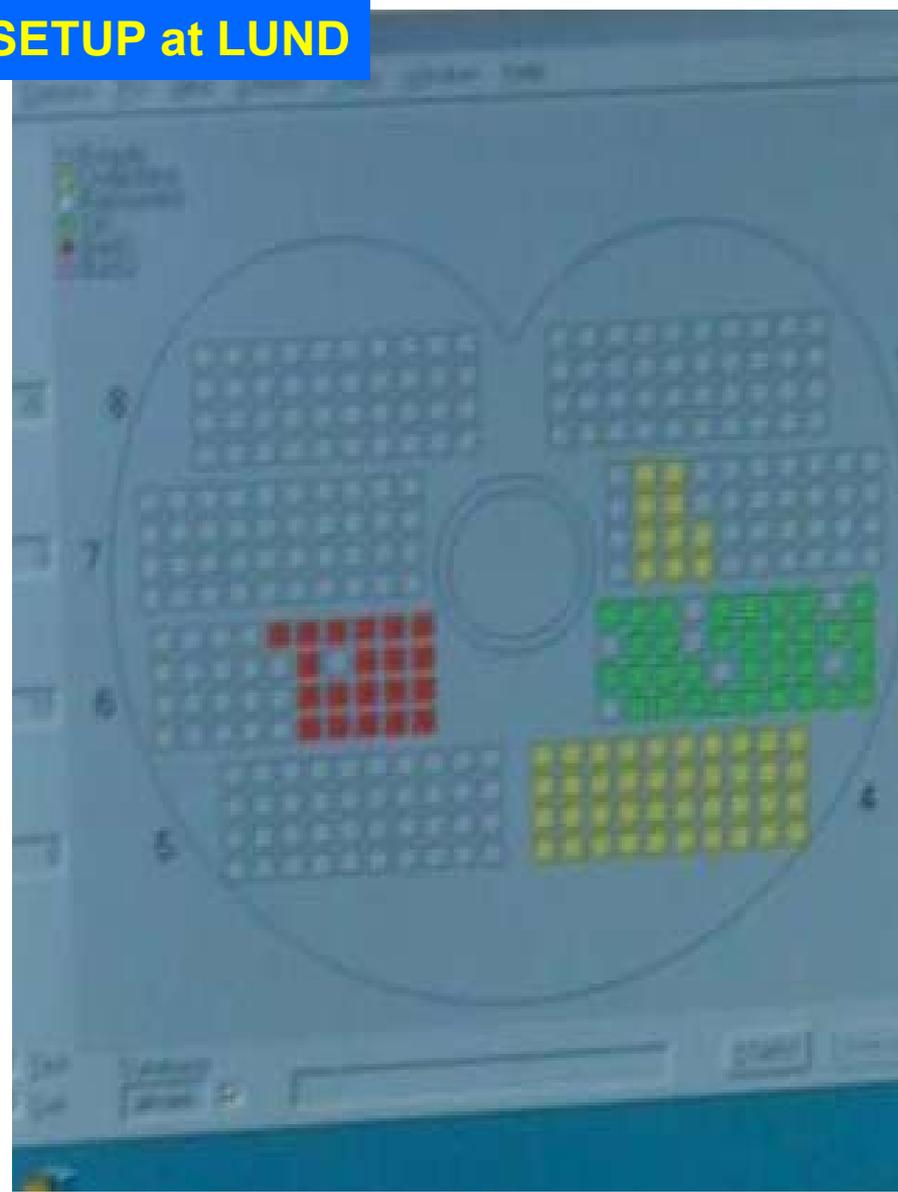
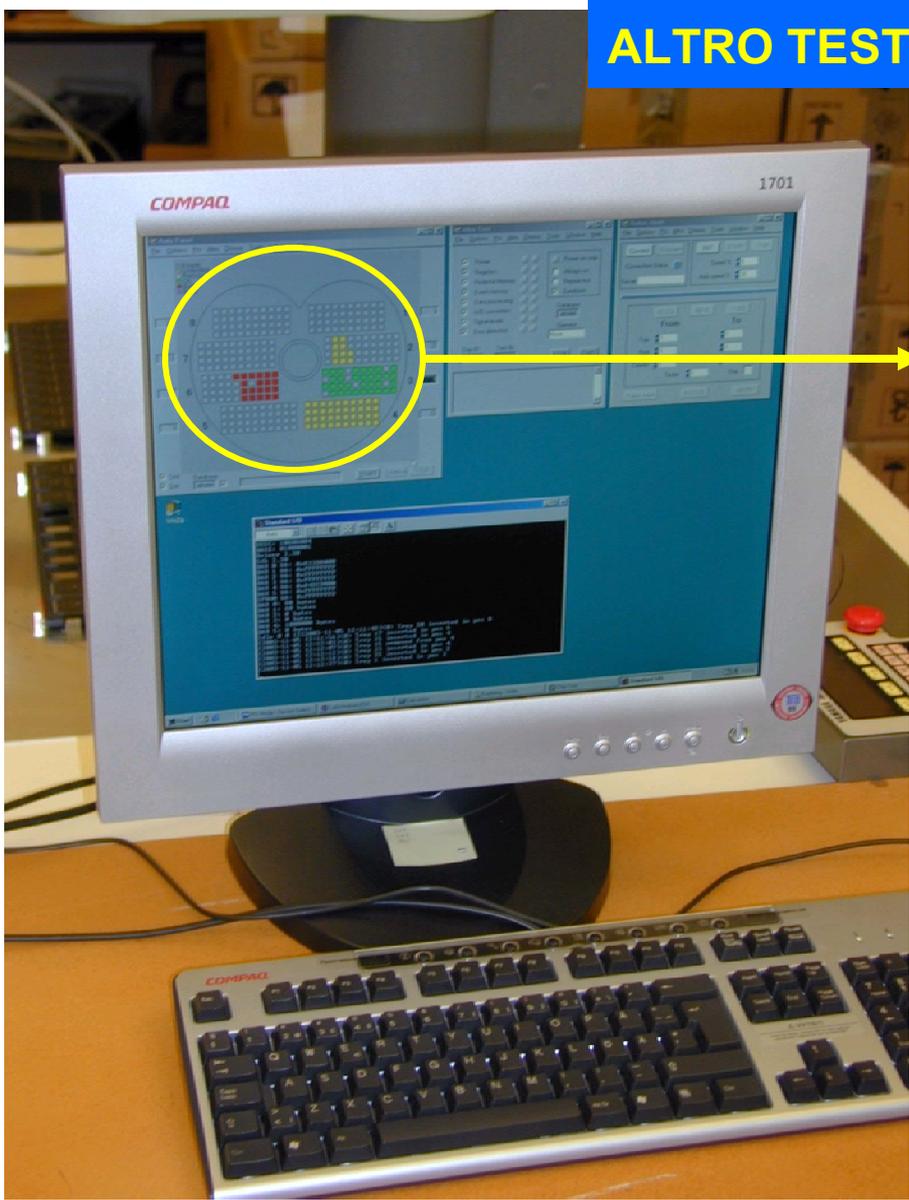
ALTRO Mass-Testing

ALTRO TEST SETUP at LUND



ALTRO Mass-Testing

ALTRO TEST SETUP at LUND



ALTRO Mass-Testing

Example - Distribution of digital Current



$$9 < I < 200$$

The majority of the chips are rejected for bit-stuck in the digital circuit

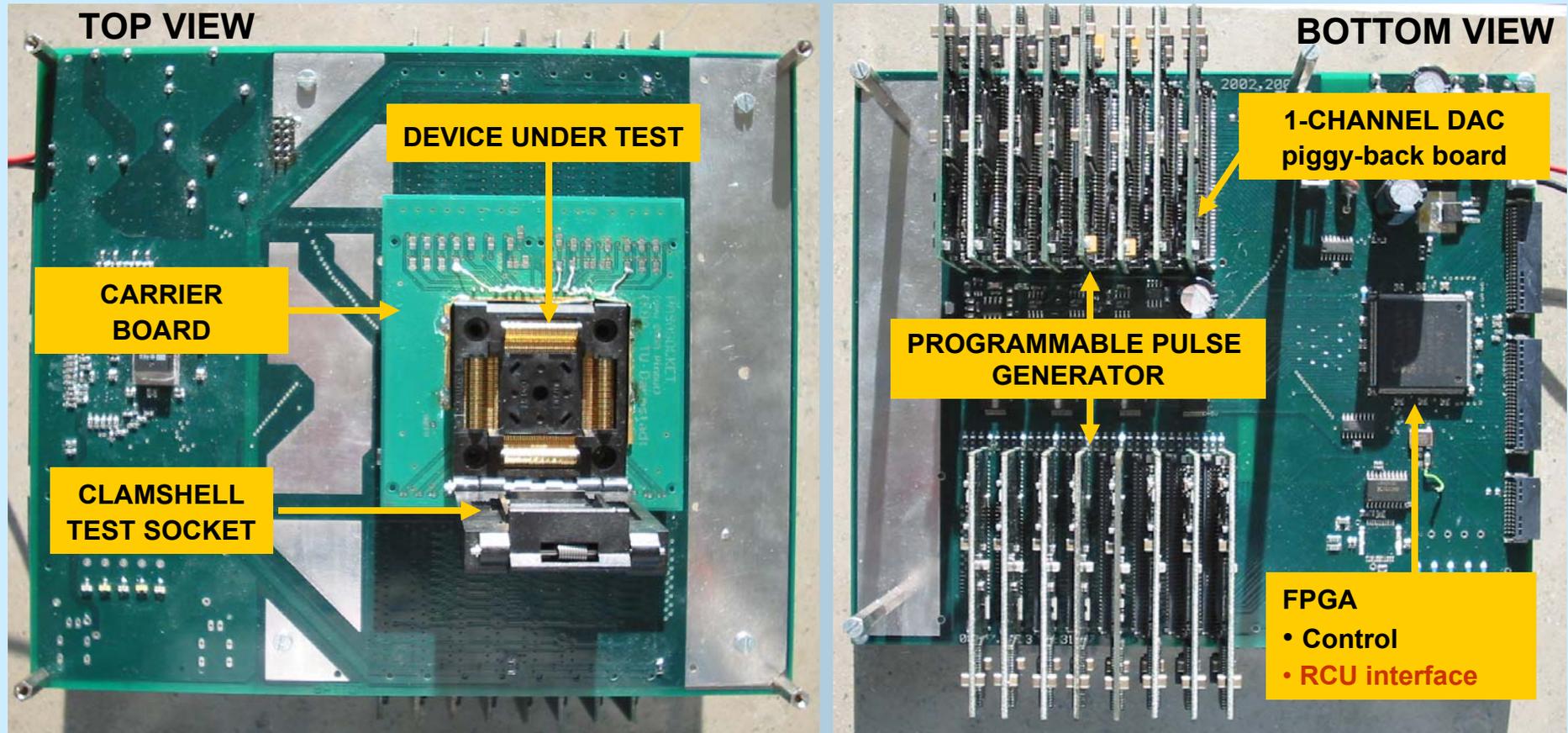
Summary

- As of Yesterday 39 000 chips tested
- Yield of directly accepted chips is 82.5 %
- Testing of remaining 6000 chips and reverification of rejected chips (~7500) will be completed by March 15
- At present, test rate of about 1000 chips a day

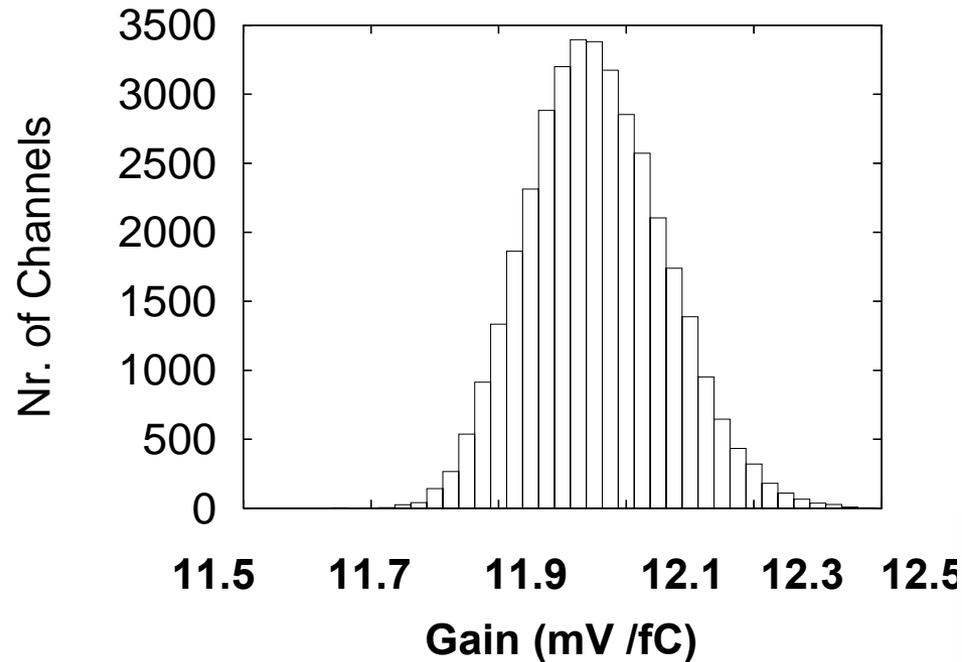
PASA Mass-Testing

DARMSTADT TU

TEST EQUIPMENT

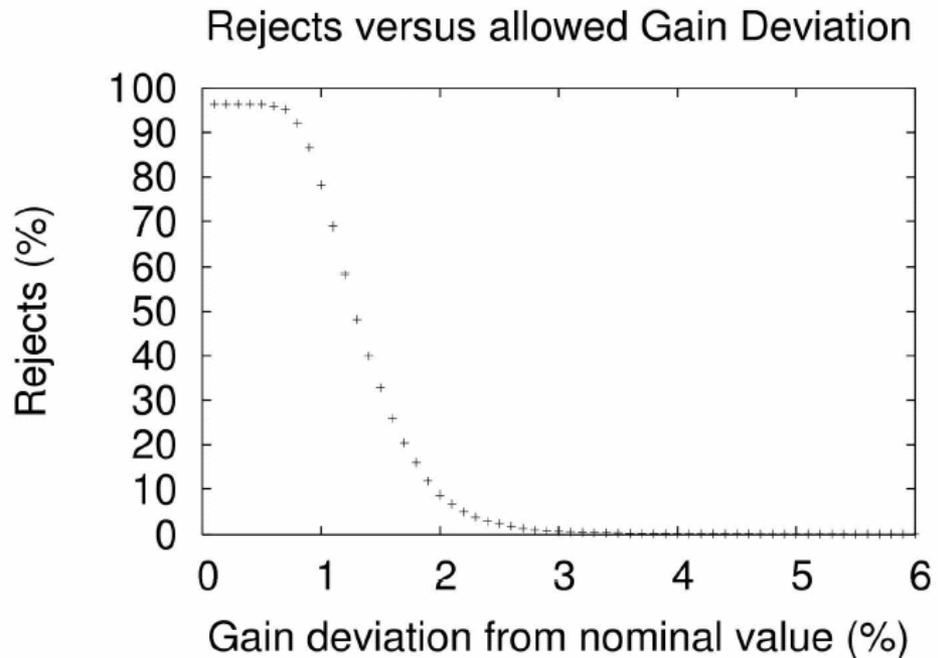


PASA Mass-Testing

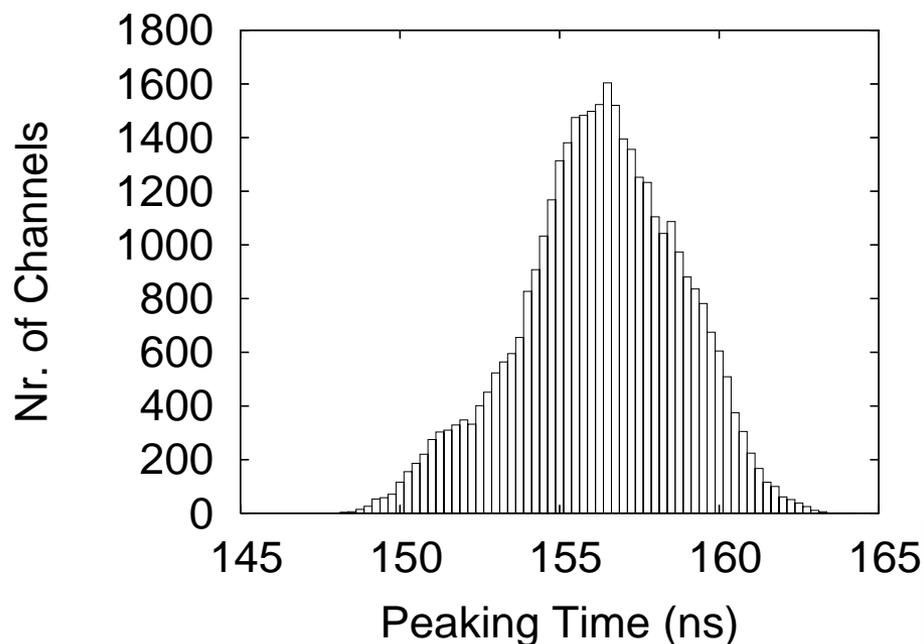


**Distribution of the Conversion Gain
measured in about 38400 channels**

**All good chips have a conversion gain
within ~3% from the nominal value**

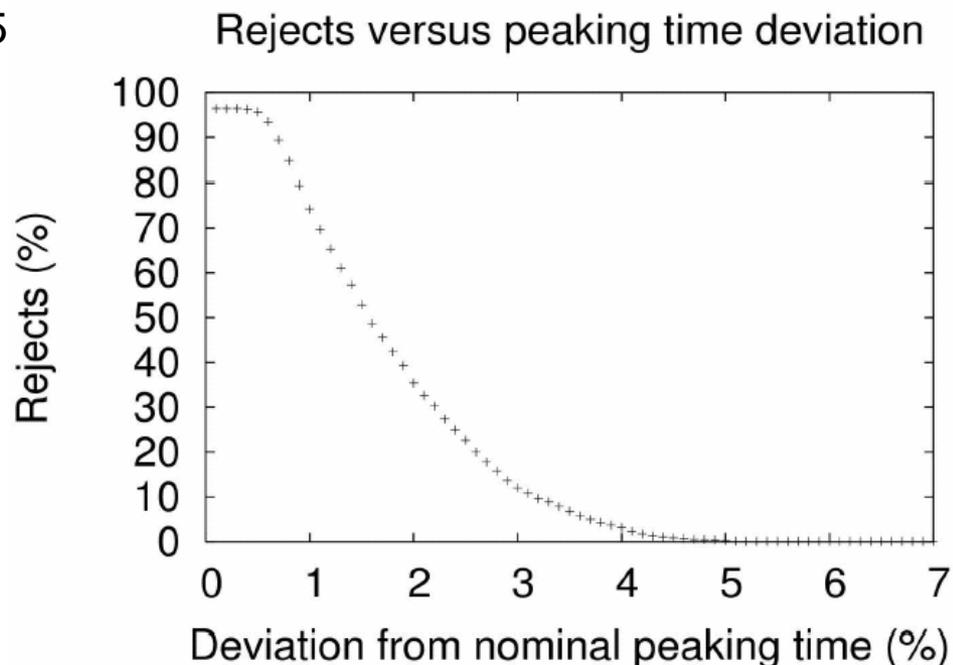


PASA Mass-Testing



**Distribution of the peaking time
measured in about 38400 channels**

**All good chips have a peaking time
within ~5% from the nominal value**



Summary

- 2500 PASAs (production lot) have been tested
- Yield of accepted chips is 96.4 %
- 55000 chips to be tested (Lund): 22 March - 30 June
- Test rate: 2 chips / minute \Rightarrow 1000 chips / day (8h)

Faulty chips

- 18 chips with high current ($> 2 \times$ nom. Value)
 - 4 chips with functional errors in all channels (large dist.)
 - 4 chips with all channels main parameters off-limits
 - 2 chips with high noise (> 1000 electrons)
 - 61 chips with gain off limits ($> 50\%$ from nom value)
-  Majority of the chips with no response