FRONT-END ELECTRONICS FOR THE ALICE TPC -DETECTOR

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Abstract

The front-end electronics for the Time Projection Chamber (TPC) for the ALICE experiment consists of $5x10^5$ channels. A single readout channel is comprised of three basic units: a charge sensitive amplifier/shaper with a fast tail cancellation; a 10 bit 10 MSPS low power ADC; a digital ASIC which contains the zero suppression circuit and a multiple-event buffer. Data from a number of channels (4096) are multiplexed into an optical link (DDL) by means of a local custom bus which can support a data throughput of 2 MByte/event at a trigger rate of 50Hz. The construction of a prototype of this electronics is presented in this paper.

1. INTRODUCTION

ALICE [1] is A Large Ion Collider Experiment now being built to study high energy heavy ion collisions at the Large Hadron Collider (LHC). LHC will collide several species of ions, ranging from protons up to lead, at centre-of-mass energy of about 5.5 TeV/nucleon.

ALICE is scheduled for initial operation in 2005. It will be composed, from the inside out, of an inner tracking system, based on six layers of high-resolution silicon tracking detectors (ITS), a cylindrical TPC, a time of flight system (TOF), an electromagnetic calorimeter and an array of counters optimised for high-momentum particle identification (HMPID). This is the central part of the detector, which covers $\pm 45^0$ over the full azimuth, embedded in a large magnet with a weak solenoidal field. The detector is completed by a forward muon spectrometer.

The relativistic ions collisions at LHC will have an extremely high charged particle multiplicity. For the central events in Pb-Pb running, for instance, about $3x10^4$ tracks will be produced in the detector acceptance. In such an environment, to achieve a good two-track resolution, is required a three-dimensional space point readout with a very high spatial granularity. ALICE uses a TPC as main tracking system.

The use of a TPC for tracking reconstruction in such high particle density environment has been shown to be possible by NA49 in the lead runs at the SPS. However, a number of ALICE-specific requirements, make new designs indispensable.

The ALICE TPC [1], of cylindrical shape, will be 500cm long, subdivided into two drift spaces of 250cm by a central high voltage plane, and extends in the radial direction from 90cm radius out to 250cm. The image charge is detected by $5x10^5$ pads located on two readout planes at the cylinder end-caps. The readout planes are based on a new concept, the Ring Cathode Chamber (RCC) [2], which makes use of a pad structure that surrounds almost completely the sense wire. In ALICE, the TPC will be used for tracking reconstruction, momentum measurement and particle identification by dE/dx.

2. ELECTRONICS REQUIREMENTS

In a TPC, the drift velocity, drift length and diffusion constant determine most of the parameters for the front-end electronics. For the ALICE TPC a cool gas mixture with a drift velocity of 2.5cm/μs and a diffusion constant of 250μm/⊠cm has been chosen as the most probable candidate.

The average longitudinal diffusion determines a shaping time of 240ns, which is comparable to the diffusion width of the detector pulse in the time domain. From the shaping time, a sampling frequency of approximately 10MHz can be derived. Thus, the total drift space of 250cm is divided into about 1000 time slots. Each of the 1000 slots corresponds to a 2.5mm drift distance.

Diffusion and electron statistics limit the resolution both in the drift and azimuth directions. Monte Carlo studies indicate that to reach the detector resolution limit, a 40:1 signal-to-noise ratio is required. The dynamic range

is set by the requirement that the electronics accommodate a 280 MeV/c proton, which is about 10 times a minimum ionising signal. To allow for Landau fluctuations, the electronics must not saturate for signals up to 20 times minimum ionising. The pad capacitance is of the order of a few pF and can integrate a maximum charge of 0.2pC (1.25×10^6 electrons), leading to a maximum acceptable noise (r.m.s.) of about 1500 electrons.

To achieve the necessary rate capability the zero suppression will be done in the front-end before the data is transferred to the DAQ system. Owing to the high channel occupancy, in order to minimise pile-up effects, a very precise tail cancellation in the front-end stage is required. To be compatible with the dE/dx resolution, a cancellation to 1‰ or better of the maximum pulse height is needed. This can be done either before or after the analogue to digital conversion.

In Pb-Pb running, event rates will reach 10^4 minimum bias events per second; in p-p running, the maximum interaction rate will be of the order of 10^5 interactions per second. A few percent of these rates correspond to central collisions that will be trigger selected. The large granularity of the TPC (5×10^8 pixels) leads to event sizes of 0.6 GByte/event. Zero suppression at the front-end will reduce the data throughput by a factor of 10; data compression at the front-end and at the DAQ will further reduce the data to the order of 2.5 GBytes/\s, with about 50 events/s written to permanent storage.

In proton-proton mode the detector will produce a data volume smaller of a factor 5.

A critical aspect in the TPC operation is the temperature stability, which influence the drift velocity. A temperature stabilisation of about 0.1°C over the whole volume, corresponding to a variation of the z-(drift) co-ordinate of 1mm in the worst case is necessary. This stability can be achieved by operating the TPC at a working temperature of 25°C and cooling the readout modules with a traditional water cooling system if the power dissipated by the front-end electronics is below 25kW (50mW/channel).

The radiation load on the TPC is low, with a total dose received over 10 years of less than 300 rad and a neutron fluency of less than 10^{11} neutrons/cm^2.

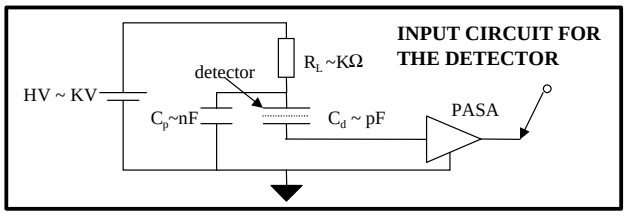
3. READOUT COMPONENTS

The front-end electronics for the ALICE TPC consists of 5×10^5 channels. A single readout channel is comprised of three basic units: a charge sensitive amplifier/shaper with a fast tail cancellation; a 10 bit 10 MSPS low power ADC; a digital ASIC which contains the zero suppression circuit and a multiple-event buffer.

3.1 Preamplifier/Shaper

The charge collected on the TPC pads is amplified and integrated by a low input impedance preamplifier (Fig.1).

Fig. 1: Input circuit for the detector.



The pulse shape of the pad signals in a TPC geometry is rather complex. It depends on the details of the chamber and pad geometry. For the RCC structure, the time dependence of the induced signal changes from the substantial undershoot behaviour [3], due to the motion of positive ions relative to the pad and the wire planes, observed in flat cathode arrangements, into 1/t tail typical of proportional tubes. This tail has to be cancelled to 1‰ or better of the maximum pulse height in about 1μs.

These analogue functions have been implemented in a custom integrated circuit, named CALICE. This circuit, that is produced in a bipolar technology (HARRIS SEMICONDUCTOR UHF1X), contains in a silicon die of 7mm^2 the preamplifier and shaper circuits for 4 channels with a power consumption/channel of 5mW.

The CALICE circuit has a input impedance ranging from 60 Ω for the dc components up to 200 Ω for the highest frequency in the range of interest, a conversion gain of 5mV/fC, an output dynamic range of 2V with a linearity of 1%. It produces a pulse with a rise time of 120ns, a shaping time (FWHM) of 240ns and a tail cancellation at the ~1‰ level after 700ns.

The single channel has a noise value (r.m.s.) below 1000 e and a channel to channel cross–talk below -60dB. The chip is supplied with 3V/-2.5 V.

3.2 A/D Conversion

Fast-conversion ADCs of the required dynamic range and precision are commercially available. Conversion times of the order of 100ns (required in our case) can be achieved with flash-ADCs or with successive approximation pipelined ADCs.

The power budget of 50mW/channel calls for low power ADCs. Fortunately, due to the explosive growth of wireless communication systems and portable devices, where the power consumption is a major problem, 10 bit 10 MSPS ADCs with low power consumption are now widely available. Fig.2 shows the trend in the reduction of the power consumption, for 10 bit ADCs, during the last 10 years. From Fig. 2 we can see that, starting from 1996, several commercial ADCs with a power consumption below 100mW are commercially available. Furthermore, most of them feature a stand-by power consumption below 10mW. In this aspect it should be noted that the ALICE TPC has a duty cycle of 10%. The digitisation occurs during the detector drift time (100 μs), triggered by the L1 decision (1KHz).

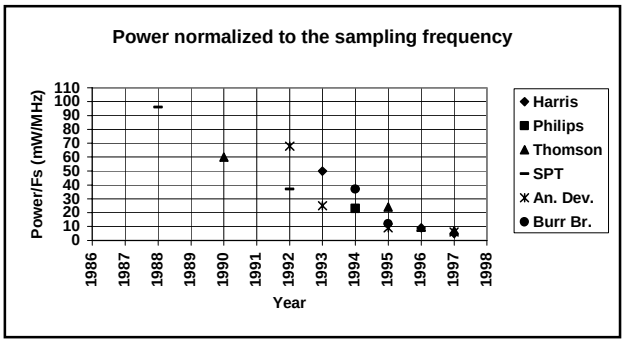


Fig. 2: power consumption versus year.

A study of 3 commercially available ADCs has been completed. Fig.3 shows the ENOB versus the frequency of the input signal. We conclude that all three fulfil the ALICE TPC requirements in terms of performance and power consumption in the frequency range of interest.

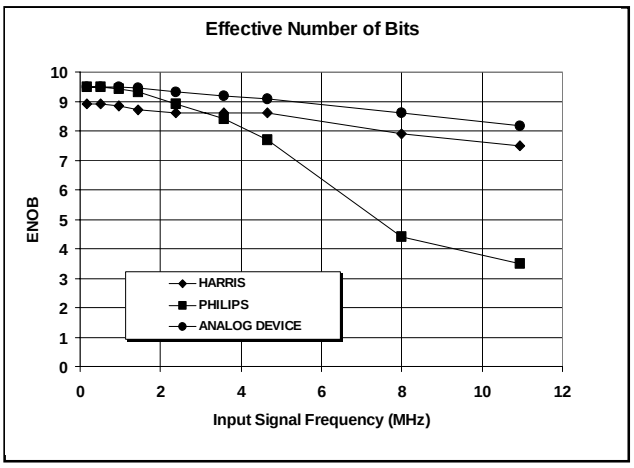


Fig. 3: ENOB versus input signal frequency

Another interesting option would be the use of a non-linear ADC. A candidate would be the CRIAD [4]. The CRIAD is a multiple-range linear ADC with 4 ranges. In each range the resolution is defined by an 8-bits linear conversion performed between two references, the upper one being the high end of the range, the lower one being ground (0V). The commutation of ranges is automatic with the signal amplitude.

3.3 Baseline subtraction, zero suppression and multiple-event buffering

The ALTRO (ALice Tpc ReadOut) chip is a custom VLSI integrated circuit. It contains the digital circuitry, for 8 channels, to perform pedestal subtraction, zero-suppression, formatting and buffering. In the block diagram of the ALTRO, shown in Fig. 4, the main logical units can be distinguished.

In the Pedestal Subtraction Unit (PSU) the lookup table (LUT) corrects any possible systematic instability of the baseline, allows the subtraction of time dependent pedestal values from the ADC samples values. Alternatively this LUT, addressed by the ADC data, can be used to perform the corrections for the non linearity of the input signal during the pedestal subtraction. Finally the same LUT can be used to generate a test pattern. That is an important feature that allows complete test of the overall digital readout chain.

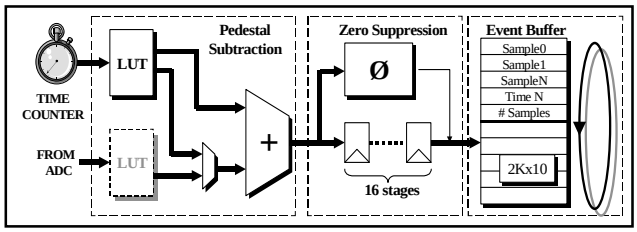


Fig. 4: ALTRO block diagram.

In the Zero Suppression Unit (ZSU) the basic pulse detection scheme implemented is based on a fixed threshold, where samples of a value smaller than some constant decision level above the baseline (threshold) are rejected. To reduce the noise sensitivity, a glitch filter checks for a consecutive programmable number of samples above the threshold. In order to keep enough information for further feature extraction, a programmable sequence of pre-samples and post-samples are also recorded. Finally, the merging of two subsequent sets, closer than 3 samples, is foreseen. The implementation of this zero suppression scheme requires 16 pipeline stages. With this pipeline a programmable number (up to 16) of samples before the trigger (pre-trigger samples) can be stored. This feature allows the compensation of the L1 to L0 trigger latency (1.6 μs).

The zero suppressed data is formatted into 32 bit words according to a back linked data structure.

L1 related data is stored in a multiple-event buffer. The Event Buffer Unit (EBU) can work both either as a fixed-length event buffer or as a variable-length event one. In the first case, a programmable amount of memory is allocated to each event independently of the event size; while in the second configuration each event occupies the memory space necessary to store the zero-suppressed event data. The first configuration clearly uses the data memory space inefficiently, while it has the advantage that front-end electronics does not need to propagate a "busy" signal to the TRIGGER/DAQ system.

The ALTRO chip interfaces to the external world through 4x10 bit ports, for the data coming from 8 dual ADCs, and a 40 bit control bus based on an asynchronous handshake protocol which can support a data transfer of 100 Mbytes/sec.

In order to have an estimation of the size and the power consumption, this circuit has been studied using the standard cell library of a 0.5μm CMOS process, leading to a die size of 8mm^2/channel and a power consumption of 8mW/channel. The production of a prototype in a MPW run is foreseen for the near future. An FPGAs

implementation of the same circuit has been designed and is now used for the readout of the TPC prototype.

4. SYSTEM DESCRIPTION

A schematic diagram of the system components and their interconnection is shown in Fig. 5.

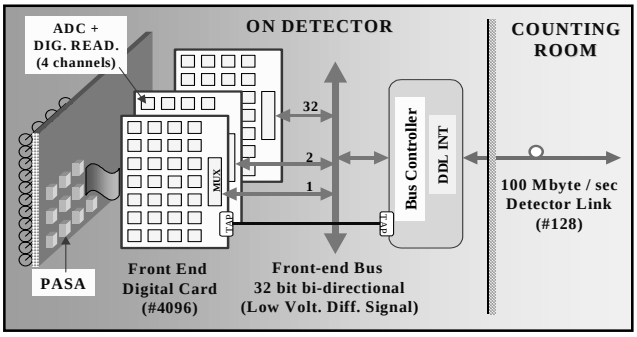


Fig.5: System block diagram.

The CALICE chips are bonded directly onto the backside of the readout plane, which houses the pad structure on its front side, using the Tape Automated Bonding (TAB) process [5]. The rest of the readout chain is contained in the front-end cards (FECs), which are plugged in crates, attached to the detector mechanical structure. Fig. 6 shows the configuration used for the prototype described in the next section.

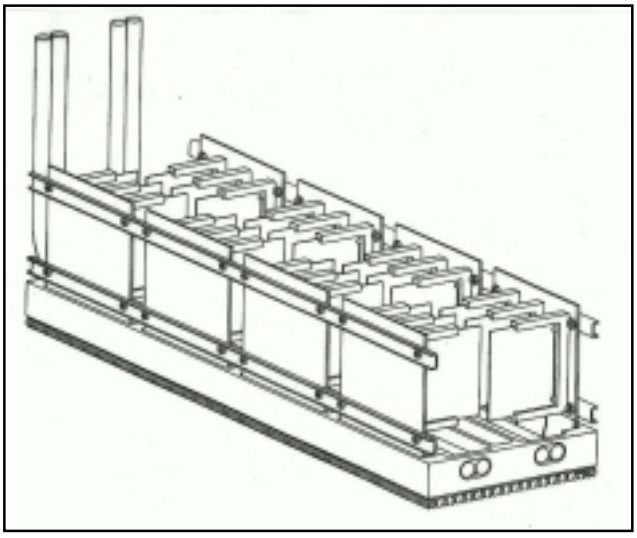


Fig.6: System mechanical structure.

Each FEC contains 128 channels. 32 FECs are controlled by a "data routing module" (DRM), which interfaces the FECs to the DAQ, the Trigger and the Detector Control System (DCS). The DRM broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via a custom bus, based on the LVDS technology. The transfer of data words is synchronous and modules containing valid unread data are enabled to assert data on the bus by individual addressing. The interfacing of the DRM modules to the Trigger and to the DAQ follows the standard data acquisition architecture of the experiment [6]. The DRM modules also provide buffering of data and word counts. Data are finally moved via the LVDS bus to the FIFO driver of the optical link.

The readout of one event is performed in two separate phases, which are consecutive for a given event, but can otherwise be activated concurrently. In a first phase the trigger information is received by the TTC system [7] and broadcast to all modules in the subsystem starting the digitisation of each channel which lasts for the detector drift time. During this phase pedestal subtraction and zero suppression are performed. In the second phase, information is moved from the output buffers to the DAQ readout receiver cards via the optical link. The time needed to complete the second phase depends on the size of the event, but other triggers can be processed during the readout of previous event, as long as the multiple-event buffers in the FEC are not "nearly" full. Dead time can be generated (by sending an "XOFF" signal to the trigger in the variable length scheme) only when this condition occurs.

5. A 2000 CHANNELS PROTOTYPE

An important milestone in the design of the large TPC is the construction of a small prototype (~2000 channels) which will be installed in the NA49 experiment during '98. The front-end electronics for the prototype TPC is designed to incorporate the main features of the electronics for the full-size detector.

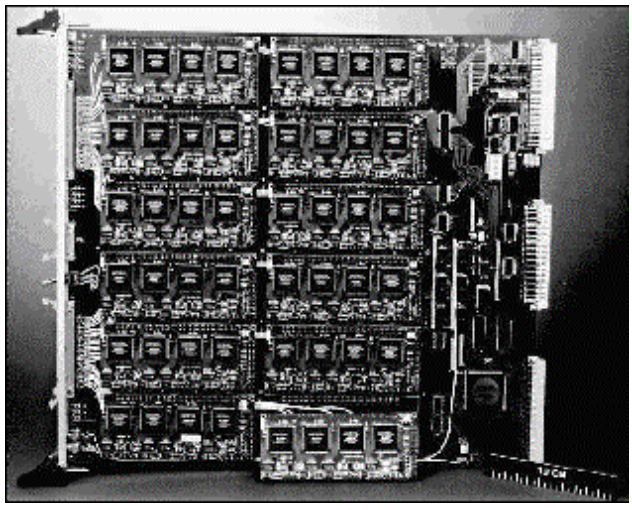


Fig.7: FEC implemented as VME board.

The realisation of the final set-up structure will be accomplished in two phases. In a first phase only the amplifier/shaper (PASA) chips will be installed close to the detector, directly mounted on the back-side of the TPC PC board, using the Tape Automated Bonding (TAB) process. The rest of the readout chain will be housed in VME units (Fig. 7) (large format) 3 meters away from the detector (Fig. 8).

This has been done to allow the testing, during the first phase, of the detector and the new electronics chain, with the standard VME.

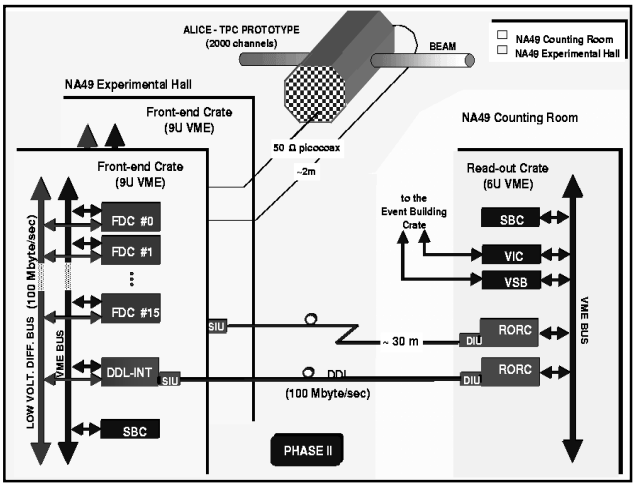


Fig. 8: FEE for the Alice TPC prototype

That has been considered as very important during the debugging phase of the prototype. In the second phase, the VME crates will be removed and new FECs will be placed close to the detector.

The amplifier/shaper chip used in the prototype is a version preceding the one above described. The main difference concerns the rise time that is of 50ns instead of 120ns [8]. For this rise time value the bandwidth limitation at about 4MHz, shown by one of the ADCs studied (Fig. 3), becomes important [9].

The ADC used in the prototype is the AD9200 (Analog Devices). The digital readout, including the pedestal LUT and the data memory, is implemented in the FPGA EPF10K20-TC144 (ALTERA). The board control logic, the VME interface and the LVDS bus interface are implemented in the FPGA EPF10K20-RC240 (ALTERA).

6. CONCLUSIONS

The ALICE TPC Front-End Electronics requires the development of two ASICs: a preamplifier/shaper circuit; a digital circuit to perform the pedestal subtraction, zero suppression and event buffering. The two ASICs, which fulfil the specifications, have been developed. ADC's according to the ALICE-TPC requirements are commercially available; however, a custom CMOS ADC, such the CRIAD, might represent an interesting solution to be further investigated. The multiplexing of a high number of front-end channels is achieved via a custom bus based on the LVDS technology. Test of a sizeable amount of this electronics in the NA49 (SPS) environment is underway.

7. REFERENCES

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