PASA Production Acceptance Test

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1 Introduction

The purpose of the production acceptance tests is to sort out and qualify the PASA chips that comply with the *Alice TPC PASA Technical Specifications* [1].

The test system adopted for the acceptance tests of the PASA chips is largely based on the same components employed in the test system for the ALTRO chip [2]. The main difference between the two systems is represented by the Chip Tester.

The architecture and the main components of the ALICE TPC front-end electronics are described in [3], while a detailed description of the PASA chip can be found in [1].

This document mainly deals with the system and procedures employed for the mass production test of the PASA chips. Section 2 describes the test system, Section 3 deals with the test algorithms and procedure, Section 4 briefly describes the various components of the test software and Section 5 focuses on the results obtained in the mass production tests of the PASA chips for the ALICE TPC. It should be noticed that the considerations made in Section 5 of the ALTRO Production Acceptance Test document [2], related to the chip handling, apply also to the test system for the PASA chip.

2 Test System

As already mentioned in Section 1, the test system for the mass production test of the PASA chip is similar to the production test system for the ALTRO chip. The main difference is represented by the Chip Tester, which is different for the two systems. Figures 1 and 2 show respectively a schematic diagram and a photograph of the system for the mass test of the PASA chip. The main components of the test system are: the *Chip Tester*, the *Robot*, a *Control PC*, a *Database PC*, an oven and a pen-plotter. The *Chip Tester* is the circuit that hosts the chip under test, stimulates all input signals and measures its response by acquiring all output signals. It will be described in section 2.1, while for a description of the other components we remand the reader to [2].

2.1 The Chip Tester

The Chip Tester has been conceived and designed to be modular and general purpose. A simplified block diagram and a photograph of the tester are shown respectively in figures 3 and 4. From the functional point of view, the Chip Tester comprises six main blocks: 1) A *Stimuli Memory*, where the stimuli for the PASA chip are stored as digital pattern; 2) a 14-bit, 40-MHz Digital to Analogue Converter (DAC), which converts the discrete-time digital signals generated by the Stimuli Memory into continuous-time analogue signals, which is input to the device under test; 3) the socket to host the device under test; 4) a 12-bit, 40-MHz Analogue to Digital Converter (ADC); 5) a memory to acquire the output signals of the device under test; 6) an interface and control circuit, which distributes all control and timing signals and implement the interface to an acquisition PCI-card, the PCI-RCU [4].

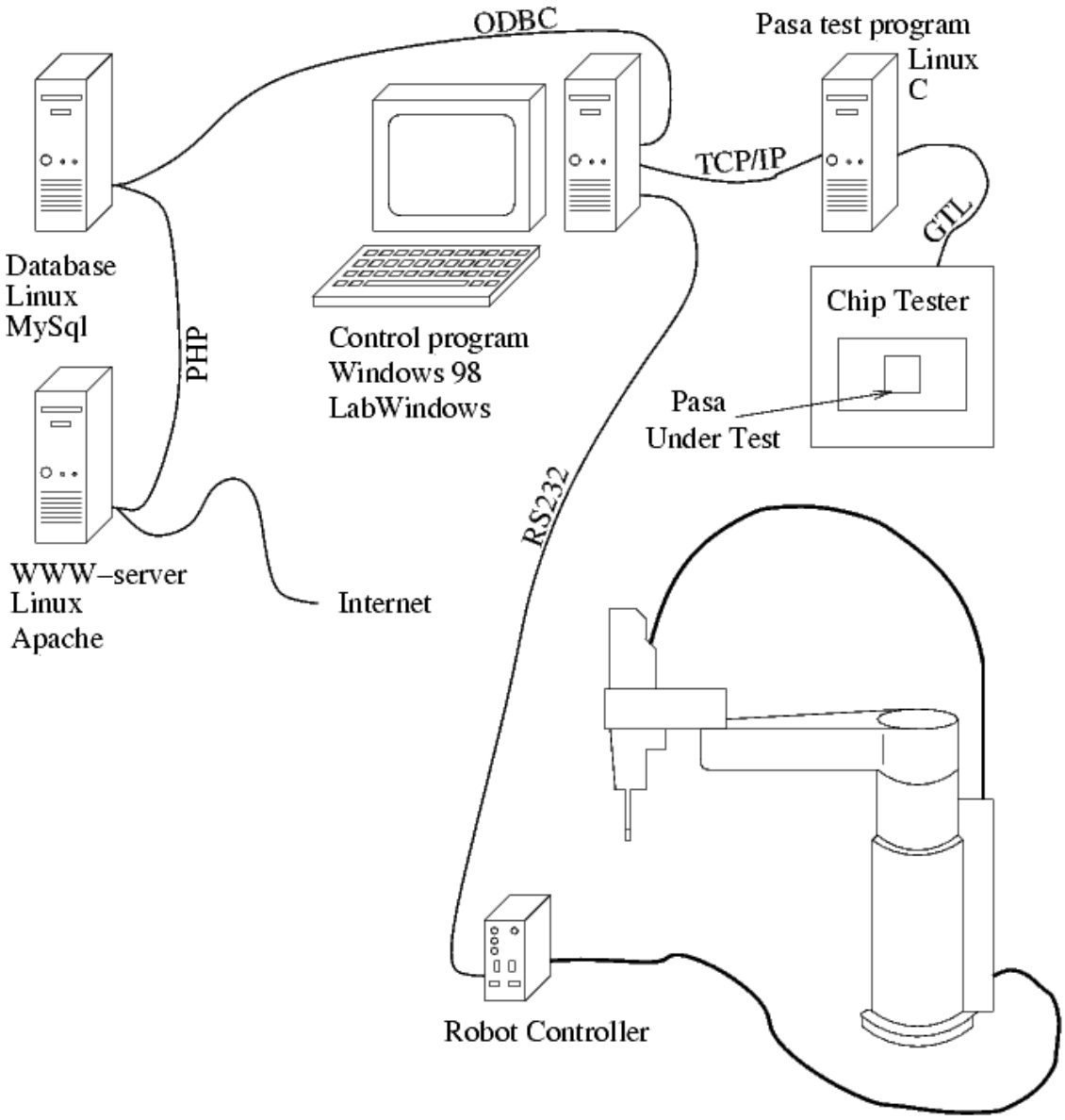

Figure 1. Schematic diagram of the production test system for the PASA chip.

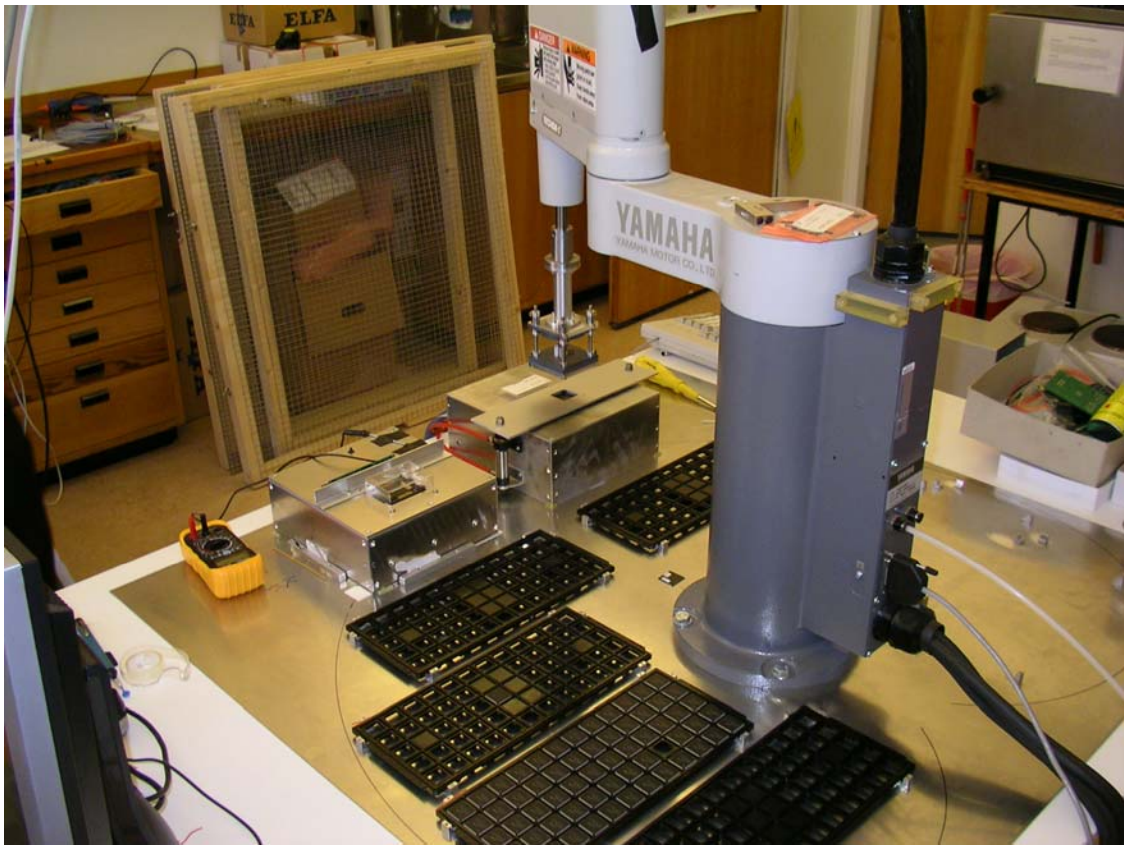

Figure 2. Photograph of the production test system for the PASA chip.

From the physical point of view, the *Chip Tester* consists of a mother board, 8 daughter cards for the generation of the stimuli (Stimuli Daughter Card), 8 daughter cards for the acquisition of the PASA response (Acquisition Daughter Card), and a daughter card that carries an open top test socket to house the chip under test.

The mother board incorporates the following circuits: an FPGA, which implements all control functions and the interface to the PCI card; the bus transceivers that electrically interface the *Chip Tester* to the PCI card; the power regulators; a 12-bit DAC that allows to define various settings for the PASA reference voltages (V_{top}, V_{bottom} and V_{common}); a set of 12-bit ADCs and a number of auxiliary circuits that allow to sense and measure the voltages and currents supplied to the device under test, and the voltages of all PASA outputs.

The Stimuli Daughter Card, which incorporates two channels, implements the stimuli memory and a 12-bit 40-MHz DAC (Burr-Brown DAC904). The board outputs two current signals (20mA full scale). These signals are terminated with a resistor to ground, thus producing a voltage signal, and connected to the PASA inputs via a series capacitor (1pF). The charge signal produced at the PASA inputs has a full-scale amplitude of 250fC. The termination resistors and the series capacitors are part of the daughter card that carries the device under test. An equalization of the gains of the different channels within 1% was achieved by means of a reference charge sensitive amplifier and a spectroscopic ADC.

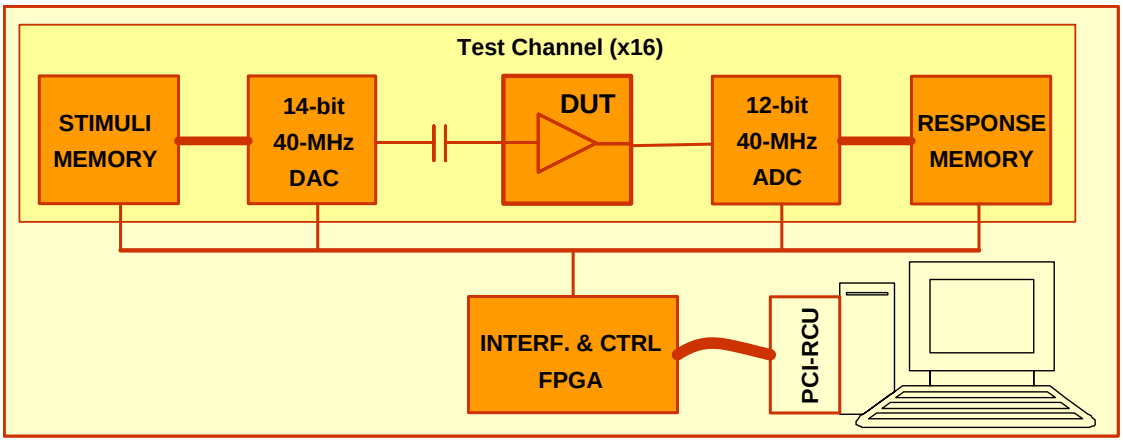

Figure 3. Block Diagram of the PASA Chip Tester.

The Acquisition Daughter Card, which also incorporates two channels, implements the digitization and the acquisition memory. The digitization is performed by two 12-bit 40-MHz ADCs (STMicroelectronics TSA1201).

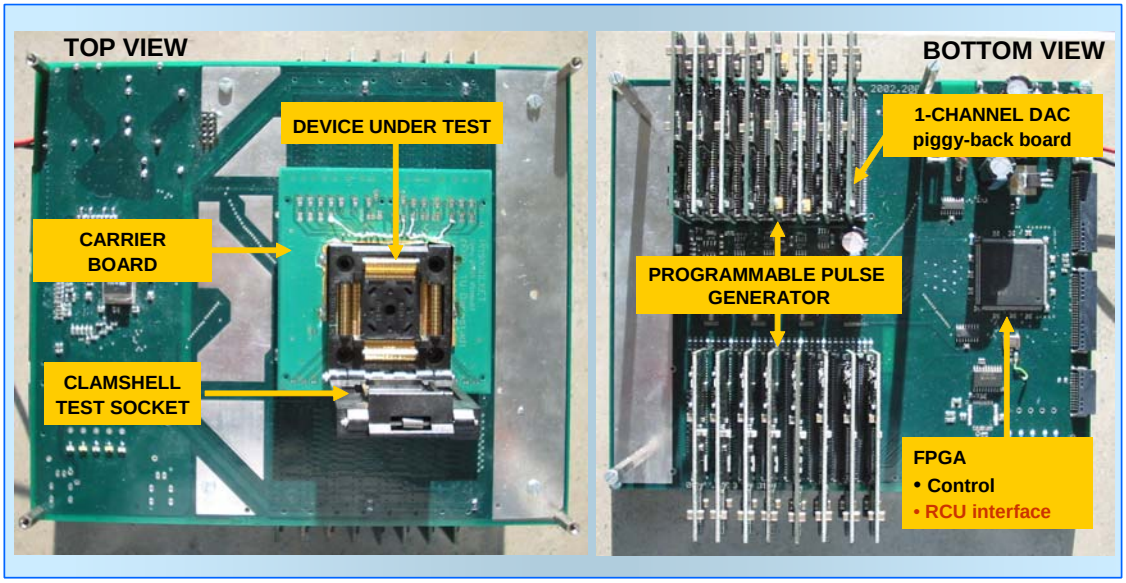

Figure 4. Photograph of the PASA Chip Tester.

A crucial aspect of the Chip Tester is the reliability of the contacts between the pins of the device under test and the leads of the test socket. This aspects has been optimized by the evaluation of several test sockets and the development of a reliable insertion mechanism. The result is a spring loaded socket mounted on a carrier board. A custom made mechanical device operated by compressed air and controlled by a PC, releases the socket to remove the chip at the end of the test. The experience, made with the test of the PASA chips for the ALICE TPC, showed that after about 35000 insertions the test socket has to be replaced.

3 Test procedures

The post-fabrication tests are performed to detect the small percentage of devices that are faulty, as a result of various defect mechanisms present in the fabrication and packaging process. This involves identifying the correctly functioning devices, but not characterising their dynamic performance. The test of the PASA chip comprises four phases: 1) the burn-in; 2) marking; 3) power test; 4) functional test. This section describes these four phases.

3.1 Burn-in

The chips are delivered by the manufacturer in plastic trays, each containing 60 chips. Prior to any electrical or functional test, all chips undergo a thermal stress cycle inside an oven. The procedure consists in placing the chips in an oven, without removing them from their trays, rising the temperature till 120^{o}C, keeping this temperature for a period of 12 hours and lowering the temperature again to 25^{o}C. This temperature cycle is executed twice. It should be noticed that the chips are not removed from the trays and are not powered. This procedure makes visible the large majority of the manufacturing defects that otherwise would appear after a long continuous operation of the device.

3.2 Marking

After the burn-in, the chips are marked with a serial number. During this operation, which is executed by a modified pen-plotter, the chips are still kept in the carrier trays. The chips trays themselves are also marked with a serial number. In the database, the chip serial number, the tray serial number and the position of the chip in the tray are recorded. In this way, we can always trace back the production lot and wafer to which the chip belongs, the tray in which the chip is stored and its location in the tray. Conversely, given a tray number we can produce the list of chips it contains, and their status.

3.3 Power and I/O Static Voltage test

After the marking, the acceptance test starts with the verification of the power consumption of the chip. An “on board” voltage regulator, equipped with the ON/OFF feature, supplies the chips under test. Therefore to insert and remove a new set of chips, the test board does not need to be completely power-down; only the board sector where the chips are being plugged undergoes the power cycle. The test-board controller, implemented in the FPGA, controls the voltage regulator. The latter has been tailored such that the maximum current it can deliver does not destroy (fuse the bonding wires) the chips under test. In this way, the nominal value of the supply voltage can be immediately applied to the chips. This circuit can measure the current absorbed by the chip. The measurement of the current is done in static conditions for the three values of the supply voltages, which correspond respectively to minimal, typical and maximal rating conditions. If the value of the power consumption is out of the acceptance range (20% of the nominal value) the chip is considered defective, the test is terminated and the chip rejected as non functional.

If the power test has a positive result, the test continues with the verification of the static voltage of all input/output pins of the PASA. If the voltage of any pin is out of range, the test is terminated and the chip rejected as non functional.

3.4 Functional Test

The chips that have passed the power and I/O static voltage test undergo two functional tests. These tests aim at measuring all characteristic parameters of the circuit: noise, conversion gain, peaking time, linearity, channel-to-channel cross-talk. The sequence of stimuli applied to the chip and the algorithms employed for the calculation of the aforesaid parameters are discussed hereunder.

The functionality of the PASA chip is verified by injecting a given charge into the 16 inputs, one at a time. The amount of charge varies over 400 different values. Each time all 16-output signals are measured. The full set of tests is performed for 3 values of the supply voltages. From these measurements the following parameters will be derived:

1. Output DC Offset
2. Conversion Gain
3. Equivalent Noise Charge
4. Linearity
5. Shaping Time
6. Channel to channel cross talk

The charge signal is created by sending a rectangular pulse into a capacitor (~1pF) in series with the input of the amplifier. The amount of charge injected takes the values $(4.8 + 0.18 \times I)$ fC with I = 0, 1, 2, …, 400, which corresponds to about half of the PASA's dynamic range. The PASA output signals are converted by the 12-bit 40-MSPS ADC, and eventually stored in the local memory for further readout.

The first step consists in measuring the output signals while the inputs are closed to ground. From this data sample, the DC offset of all the channels can be obtained.

The second step consists in injecting the charge signals in the amplifier's inputs, one at a time. Each input rectangular pulse creates an output semi-gaussian pulse whose amplitude is proportional to the charge of the input signal. In order to extract the amplitude and the full-width-half-maximum information, the digitised pulses have to be reconstructed with a Gamma-4 fit. From each reconstructed pulse we extract two numbers:

- A: amplitude;
- W: width (FWHM)

We use 3 indexes to refer to these two quantities measured for the different input pulses and channels. The first two indexes - n and m (n, m = 0, 1, 2, …, 15) - refer to a measurement of the output pulse in channel n when the input pulse is injected in channel m. The third index j (j = 0, 1, 2, …, 400) refers to the amplitude of the input signal. The following numbers will be derived for each chip:

A_{nnj}, W_{nnj}: n = 0, 1, 2, …, 15; j = 0, 1, 2, …, 400;

A_{mnj}, W_{mnj} m, n = 0, 1, 2, …, 15; j = 400;

- The value of the amplitudes divided by the corresponding input charge gives the conversion gain:

$$\text{Conversion gain} = A_{nnj}/Q_j$$

- The standard deviation of the distribution of the amplitudes, divided by the conversion gain, gives the noise:

$$\text{Noise} = \sqrt{E[((A_{nnj} - \langle A \rangle_{nj}) / \text{conversion gain})^2]} \quad j = 0, 1, \ldots, 400;$$

- The mean value of the FWHM is computed using all the measurements:

$$FWHM_n = E[W_{nnj}] \quad j = 0, 1, 2, \ldots, 400;$$

- To compute the linearity, the amplitudes of the output signals corresponding to the 400 different input signals are linearly fitted. The mean squared error between the best linear fit and the sample of measured amplitudes will be taken as measurement of the linearity.

For simplicity, the chips are sorted, according to the test results, in three classes: functional, out-of-tolerance and non functional. A chip is *non-functional*, if the power consumption or any of the characteristic parameters deviates more than 20% with respect to the average values. For the ALICE TPC acceptance test the following criteria were adopted to define the functional chips:

- Conversion gain within ±5% with respect to the mean value;
- Peaking time within ±6% with respect to the mean value;
- Output offset voltage of all channels within 50mV with respect to the mean value.

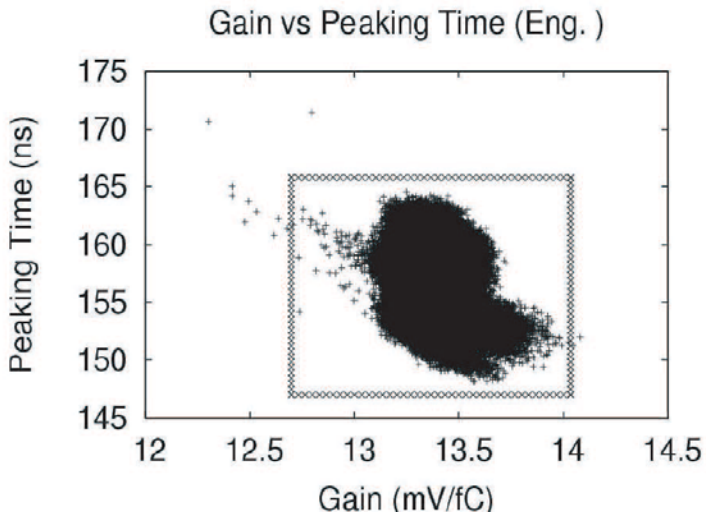

Figure 5. Distribution of the Conversion Gain versus peaking time and the selection criteria as line

Figure 5 shows the distribution of the conversion gain and peaking time together with the lines defining the chosen selection criteria. The peaking time, which as already mention is calculated with a Gamma-4 fit, is proportional to the shaping time. Testing one chip requires about 15 s for the various motions of the robot and about the same time to run the test program, leading to a test rate of 2 chips per minute.

In Figure 6 the response of a typical channel is shown for a sequence of increasing charge pulses over the full time range (left side) and an expanded view of the highest peak with a fit to a Gamma-4 function (right side). From this information the deviation from linearity is extracted by fitting a straight line to the response of the PASA (Fig. 7, left side). The deviation from a linear behaviour is shown on the right side of Fig. 7. Three different methods were used to extract the amplitudes: the maximum from the Gamma-4 fit, the time bin with the highest amplitude and the integral of the signal. Systematic differences between the different methods can be observed. Nevertheless the linearity is well within the required limit of 0.3%.

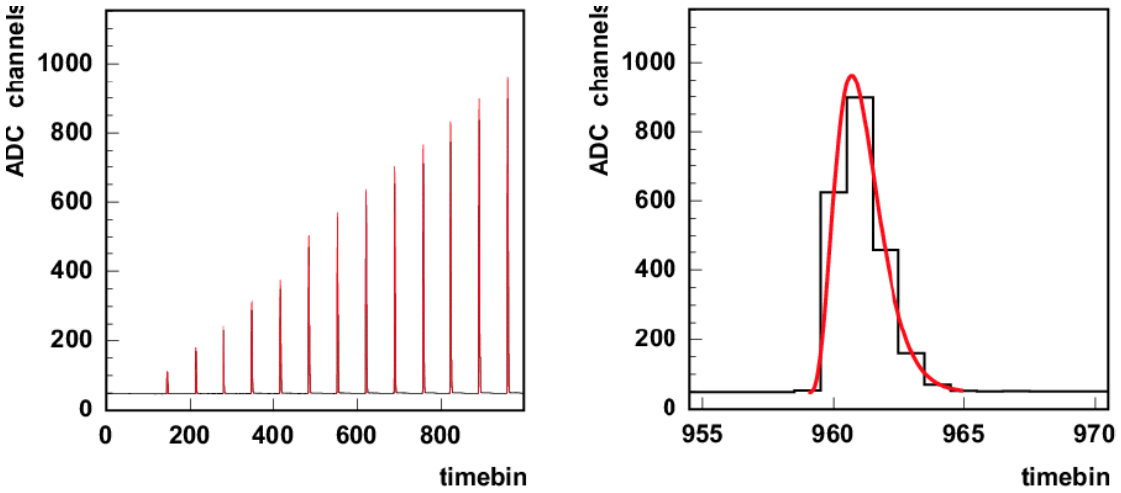

Figure 6. Sequence of pulses with increasing charge (left side). Blow up of the highest peak together with a Gamma-4 fit (right side).

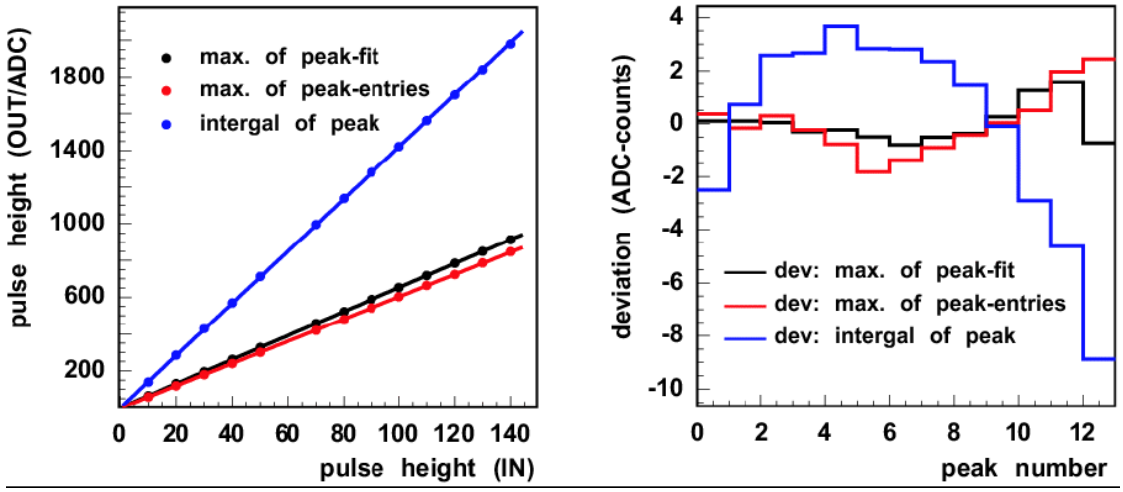

Figure 7. Determination of linearity for a typical channel. Different methods to determine the amplitudes are compared.

3.5 Selection Criteria

The acceptance criteria are to be defined such that the functional chips comply with the PASA technical specifications described in table 1.1 of [1]. However, as it has been done for the ALICE TPC production acceptance tests, more stringent criteria can be applied to select a sample of *functional* PASA chips with a narrower dispersion of ENC, conversion gain, peaking time, output DC voltage and power consumption.

4 Software

The operation of the tests and the analysis of the results are preformed under the control of a test program that runs in a LabWindow environment.

The API consists of three packages. A first package (Test Operation Program) controls the execution of the test, i.e. the operation of the Chip Tester and the analysis of the results. A second package (Robot Control Program) controls the motion of the robot and the sorting of the chips according to the test results. The third package (Database Access Program), which controls the access to the database, is used to record, retrieve and update the test results and some comprehensive statistical information. The Robot Control Program and Database Access Program are the same developed for the operation of the ALTRO Production Acceptance Test System [2].

The Test Operation Program implements the configuration, control and readout of the Chip Tester. It runs on a dedicated Linux PC, which hosts the PCI-RCU card, that implements the interface to the Chip Tester. The PASA's characteristic parameters are extracted from an intermediary data file using a program based on the Gnu Scientific Library.

5 Test results

In this section we summarize the results obtained in the mass production test of the PASA chips for the ALICE TPC. The chips have been produced in two runs: one engineering run, consisting of 1 lot of 6 wafers, followed, after the approval of the engineering samples, by a production run consisting of 1 lot (25 wafers). The whole production - wafer manufacturing, dicing and packaging - yielded about 50000 chips.

In total, only about 2% of all tested chips are non functional. 40855 PASA chips fulfilled the chosen selection criteria and were used for loading the FECs. The remaining 12.3% are functional but with at least one channel having characteristics outside the specifications. In most cases the chosen range of the offset voltage was exceeded. This parameter influences the dynamic range of the FECs. These PASA chips can easily be used adapting the FECs slightly. For this reason, a second test run was performed for these out-of-tolerance chips and they were sorted into three classes with different ranges of offset voltages: within a larger range of ±75 mV around the same mean value were 23% of the remaining chips. With a mean value being 1% lower than before and within a range of ±50 mV (same as for the first test) 54% were found. Finally 20% were sorted in a group with a 1% higher mean value and within a range of ±50 mV.

6 References

[1] "ALICE TPC PASA Technical Specifications", L. Musa and Hans-Kristian Soltveit., http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/pasa.htm

[2] L. Musa and Lennart Osterman, ALTRO Production Acceptance Tests, October 2005, http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc/testing.htm

[3] L. Musa et al., The ALICE TPC Front End Electronics, Proc. of the IEEE Nuclear Science Symposium, October 2003, Portland.

[4] R. Esteve Bosch et al., Proc. Of the 9th Workshop on Electronics for LHC Experiments, Colmar, September 2002.