Front End Electronics for the ALICE Time Projection Chamber

Requirements and System Overview

CONTENTS

1 Introduction

This document reviews the requirements (Section 2) for the front-end electronics of the ALICE Time Projection Chamber [1] and discusses briefly the general architecture and the basic building blocks (Section 3). Eventually the connectivity and mapping of the electronics into the readout chambers are briefly discussed in Section 4.

2 General Requirements

As detailed in [2], the front-end electronics has to read out the charge detected by 570132 pads located on the readout chambers at the TPC end-caps. These chambers deliver on their pads a current signal with a fast rise time (less than 1ns), and a long tail due to the motion of the positive ions. The amplitude, which is different for the different pad sizes, has a typical value of 7μA. The signal is delivered on the detector impedance that, to a very good approximation, is a pure capacitance of the order of few pF.

The main requirements for the readout electronics, listed in Table 1, are briefly discussed below.

- Diffusion and electron statistics limit the resolution both in the drift and azimuth directions. Monte Carlo studies [3] indicate that to reach the detector resolution limit a signal to noise ratio of 30:1 is required.

- The maximum pad and time bin for a hit corresponds typically to a charge of about 4.8fC ($3x10^4$ electrons) for a minimum ionising particle, leading to a maximum acceptable noise (r.m.s.) of about 1000 electrons.

- The ionisation to be measured in a single pad can be large. The most probable proton transverse momentum is expected to be about 550 MeV/c; 280MeV/c and 340 MeV/c protons, e.g., have about 15 and 8 times the energy loss of a MIP. Owing to Landau fluctuations, another factor 2-4 in dynamic range has to be considered. Thus, the electronics must not saturate for signals up to 30 MIP leading to a dynamic range of at least 10 bits.

- The amplifier conversion gain has to be such that the maximum output signal matches the input dynamic range of the ADC. An ADC with 2V dynamic range, e.g., requires a conversion gain of about 12mV/fC.

- In general, the shaping time has to be a compromise between, the need for achieving a high signal-to-noise ratio (bandwidth limitation) and that for avoiding overlap of successive signals. It should be noticed that, owing to longitudinal diffusion and to the track inclination, the signal spreads in time. Therefore, as soon as the shaping time becomes small as compared to the width of the pulse, the current pulses due to the different primary electrons will be visible at the shaper output. The signal width varies from 124 ns (r.m.s.), for 90^0-tracks, to 400ns (full width), for 45^0-tracks. It can be shown [4] that a shaping time of about 190ns, which is comparable to the signal width (FWHM), is compatible with the low noise requirement.

- The shaping time of about 190ns makes a sampling frequency of 5-6 MHz plausible. We therefore divide the total drift time of 88μs into about 500 time bins, leading to a sampling frequency of 5.66 MHz. Each of the 500 time bins corresponds to a drift distance of 5mm.

- Owing to the high channel occupancy, in order to minimise pile-up effects, a very precise tail cancellation, at the level of 1‰ of the maximum pulse height, in the front-end stage is required. This can be done either before or after the analogue to digital conversion.

- The TPC large granularity ($5.7x10^8$ pixels for 500 time bins) leads to event sizes of about 84 Mbyte after zero suppression (132 Mbyte for time bins of 130ns). To achieve the necessary rate capability the zero suppression has to be done in the front-end before the data is transferred to the DAQ system. In Pb-Pb running, event rates will reach 10^4 minimum bias events per second, while in p-p running the maximum interaction rate will be of the order of 10^5 interactions per second. A few percent of these rates correspond to central collisions that will be trigger selected. Zero suppression at the front-end will reduce the data volume by a factor 2.5, leading to a data throughput of 8.4 Gbyte/s (13.2 for the shorter time bins) with 100 events/s transferred to the DAQ/HLT processing. The reduction form the Level-1 rate of up to 200Hz to 100Hz after Level-2 is due to pileup protection against further interactions during the entire drift time of the TPC. Taking this into account, at least 140 Detector Data Links (DDLs) should be foreseen for the data transfer from the front-end electronics to the DAQ. In pp mode the detector will produce a data volume smaller by a factor 5.

- A critical aspect in the TPC operation is the temperature stability; to ensure a constant drift velocity it has to be controlled at the level of about 0.1^oC over the whole volume. The large number of channels (570132) requires the development of a system with low power consumption. The aim is to keep the total power consumption below 60kW (100mW/channel). We plan to remove the heat from the readout modules with a water-cooling system.

- The radiation load on the TPC is low, with a total dose received over 10 years of less than 300 rad and a neutron flux of less than 10^{11} neutrons/cm^2. Thus standard radiation-soft technologies are suitable for the implementation of this electronics. Still some special care should be taken to protect the system against potential damages caused by Single Event Effects (SEEs).

PARAMETER	VALUE
Nr. of channels	600 000
Signal-to-noise ratio (MIP)	30:1
Dynamic range	900:1
Noise (ENC)	1000 e
Conversion gain	12mV/fC
Cross-talk	< 0.3 %
Shaping time	200 ns
Sampling rate	5 MHz
Tail correction after 1μs	1‰
Bandwidth to DAQ/HLT	7 Gbyte/sec
Max dead time	10 %
Power consumption	< 100 mW / channel

***Table 1**: Front-end electronics requirements*

The front-end electronics system has to satisfy many other constraints while meeting the required performance specifications. Mainly, the read-out electronics needs to fit into the overall detector structure; in particular into the available space, which has important consequences for our requirements on reliability, power, and cooling.

The following sections provide more details on these requirements and show how we plan to meet these challenges.

3 System Overview

The front-end electronics for the ALICE TPC consists of 570132 channels. A single readout channel is comprised of three basic functional units (fig. 1): a charge sensitive amplifier/shaper (PASA); a 10 bit 10 MSPS low power ADC; a digital circuit that contains a shortening filter for the tail cancellation, the baseline subtraction and zero suppression circuits, and a multiple-event buffer.

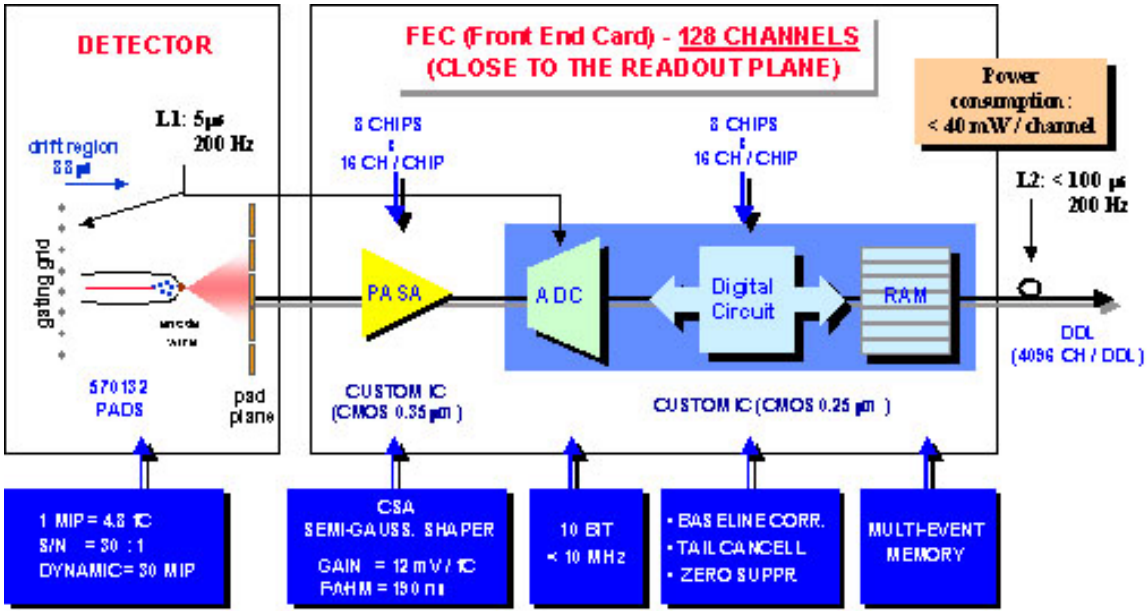

Fig. 1*: Front-end electronics basic components.*

The charge collected on the TPC pads is amplified and integrated by a low input impedance amplifier. It is based on a charge sensitive amplifier (CSA) followed by a semi-Gaussian pulse shaper of the 4-th order. These analogue functions are realised by a custom integrated circuit, implemented in a CMOS technology 0.35µm, which will contain 16 channels with a power consumption/channel of 12mW. The circuit has a conversion gain of 12mV/fC and an output dynamic range of 2V with a linearity of 1%. It produces a pulse with a rise time of 120ns, a shaping time (FWHM) of 190ns. The single channel has a noise value (r.m.s.) below 1000 e^- and a channel-to-channel cross–talk below 0.3%.

Immediately after the PASA, a 10-bit pipelined ADC (one per channel) samples the signal at a rate of 5-6 MHz. The digitised signal is then processed by a set of circuits that perform the baseline subtraction, tail cancellation, zero-suppression, formatting and buffering. The ADC and the digital circuits are contained in a single chip named ALTRO (ALice Tpc ReadOut). The ALTRO chip integrates 16 channels, each of them consisting of a 10-bit, 30-MSPS ADC, a pipelined Digital Processor and a multi-acquisition Data Memory. When a Level-1 trigger is received a predefined number of samples (acquisition) is temporarily stored in a data memory. Upon Level-2 trigger arrival the latest acquisition is frozen, otherwise it will be overwritten by the next acquisition. The Digital Processor, running at the sampling frequency, implements several algorithms that are used to condition and shape the signal. After digitisation, the Baseline Correction Unit I is able to perform channel-to-channel gain equalisation and to correct for possible non-linearity and baseline drift of the input signal. It is also able to adjust DC levels and to remove systematic spurious signals by subtracting a pattern stored in a dedicated memory. The next processing block is an 18-bit, fixed-point arithmetic, 3rd order Tail Cancellation Filter. The latter is able to suppress the signal tail, within 1µs

after the pulse peak, with the accuracy of 1LSB. Since the coefficients of this filter are fully programmable, the circuit is able to cancel a wide range of signal tail shapes. Moreover, these coefficients can be set independently for each channel and are re-configurable. This feature allows a constant quality of the output signal regardless of ageing effects on the detector and/or channel-to-channel fluctuations. The subsequent processing block, Baseline Correction Unit II, applies a baseline correction scheme based on a moving average filter. This scheme removes non-systematic perturbations of the baseline that are superimposed to the signal. At the output of this block, the signal baseline is constant with an accuracy of 1LSB. Such accuracy allows an efficient Zero-Suppression procedure, which discards all data below a programmable threshold, except for a specified number of pre- and post- samples around each pulse. This produces a certain number of non-zero data packets, thus reducing the overall data volume. Each data packet is formatted with its time stamp and size information in a way that reconstruction is possible afterwards. The output of the Data Processor is sent to a Data Memory of 5-Kbyte, able to store up to 8 full acquisitions. The data can be read out from the chip at a maximum speed of 60MHz through a 40-bit wide bus, yielding a total bandwidth of 300-Mbyte/s. Moreover, the readout speed and the ADC sampling frequency are independent. Therefore, the readout frequency does not depend on the bandwidth of the input signal being acquired. The ALTRO chip is implemented in the ST 0.25µm HCMOS-7 process.

The complete readout chain is contained in the front-end cards (FEC), which are plugged in crates attached to the detector mechanical structure. Each FEC contains 128 channels and is connected to the cathode plane by means of 6 flexible cables. A number of FECs (up to 25) are controlled by a "Readout Control Unit" (RCU), which interfaces the FECs to the DAQ, the Trigger, and the Detector Control System (DCS) as shown in fig. 2. The RCU broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via a custom bus, based on low-voltage signalling technology (GTL), which provides a data bandwidth of 200Mbyte/s. The interfacing of the RCU modules to the Trigger and to the DAQ follows the standard data acquisition architecture of the experiment [5].

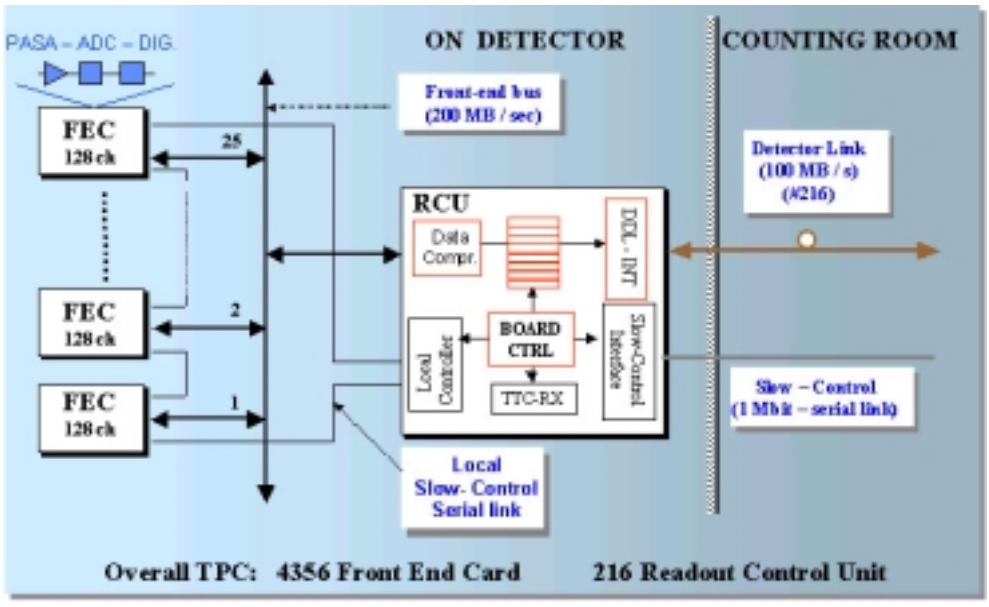

Fig.2. *Front End Electronics global architecture*

In summary, for each of the 36 TPC sectors, the front-end electronics consists of 121 FECs, 6 RCUs, and 6 detector data links.

4 Interconnection to the cathode plane

Several constraints define the mapping of the detector into front-end boards.

- The total length of the connecting wires has to be minimised.
- The cables used for this connection should be all of the same length. That should avoid the production of several types of cables and especially should guaranty the homogeneity of performance over the different detector.
- Cable crossing should be avoided to minimise the risk of error and a solution as uniform as possible should be found.

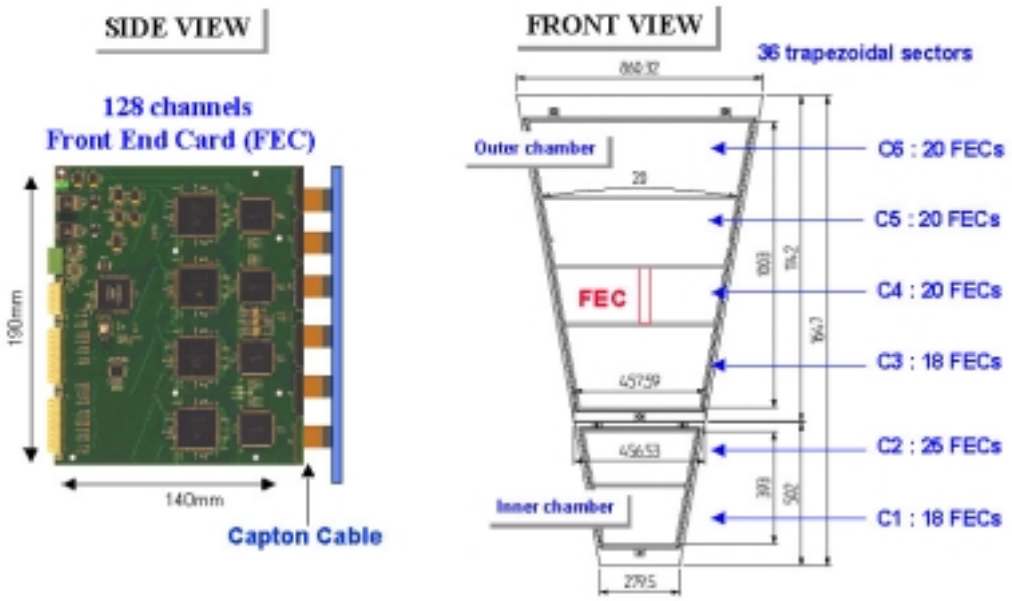

Fig. 3 *Connection of front-end electronics to the cathode plane*

These considerations lead to the interconnection scheme shown in fig.3. The signals coming from either 21 or 22 pads are grouped together and transported to the front-end cards via a transmission chain consisting of one connector soldered on the pad plane, a flexible capton cable and a second connector soldered on the FEC. The high granularity in the connectivity allows keeping sufficiently short the traces by which the signals are collected from the pads and concentrated in the area where the connectors are soldered on the pad plane (transport points). In this respect, the pads located at the top and bottom edges of the sectors, which due to the mechanical frame are not directly accessible, represent an exception. As matter of fact these pads require a longer trace.

To avoid to different types of boards, we opted for a radial disposition of the boards. The boards are grouped in 6 sets of respectively (from the inside out) n1, n2, n3, n4, n5 and n6 boards. The first two sets are connected to the pads of the inner sector of the read-out plane and are the smallest one. The next two groups are connected to the central sector pads and the last two groups are connected to the outer sector. Table 2 summarizes the numbers of boards contained in each FECs set.

The connectors used on the pad plane (F10-295 from Harwin®) are standard for vertical connection of flat flexible cables. They have 23 ways each with a pitch of 1 mm. Six connectors are grouped to connect to one FEC; two of them have 2 ground lines, 4 have 1 ground line. The FE-cables are flexible capton cables

of 7.7cm. The detailed routing and distribution of signal and ground lines is not finally decided and is subject to tests described in [6].

***Table 2**. Mapping of the front-end electronics cards.*

GROUP	NR. OF BOARDS
G1	18
G2	25
G3	18
G4	20
G5	20
G6	20

References

[1] ALICE TPC TDR, CERN/LHC 2000-01

[2] ALICE TPC TDR, CERN/LHC 2000-01, Sections 4.1.2 and 4.1.4

[3] ALICE TPC TDR, CERN/LHC 2000-01, Section 4.1.2

[4] J.C. Berset, L. Musa, M. Richter, Internal Note ALICE99-49

[5] ALICE Collaboration, Technical Proposal, CERN/LHCC/95-71

[6] U. Frankenfeld et al., The ALICE Inner Readout Chamber: Results of beam and Laser tests, http://alice-tpc.gsi.de/tpc/documents/documents.html