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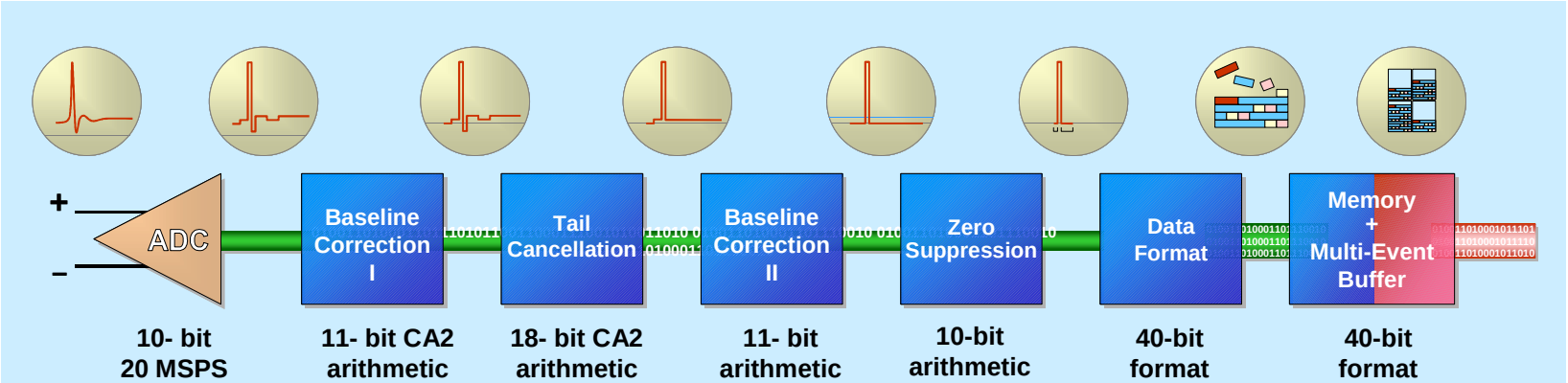
- ALTRO Test Setup and Equipment
- ADC Characterisation
- Noise and Crosstalk
- Power Consumption
- ALTRO Testing Strategy
- Functional and Physical Validation
- Yield Results and Considerations
- Conclusions

ALICE TPC READOUT CHIP (ALTRO-16)

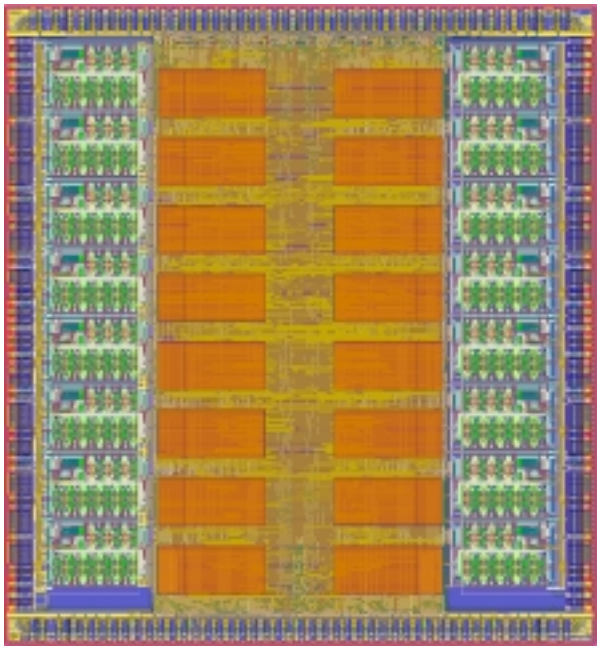


MAX SAMPLING CLOCK 40 MHz

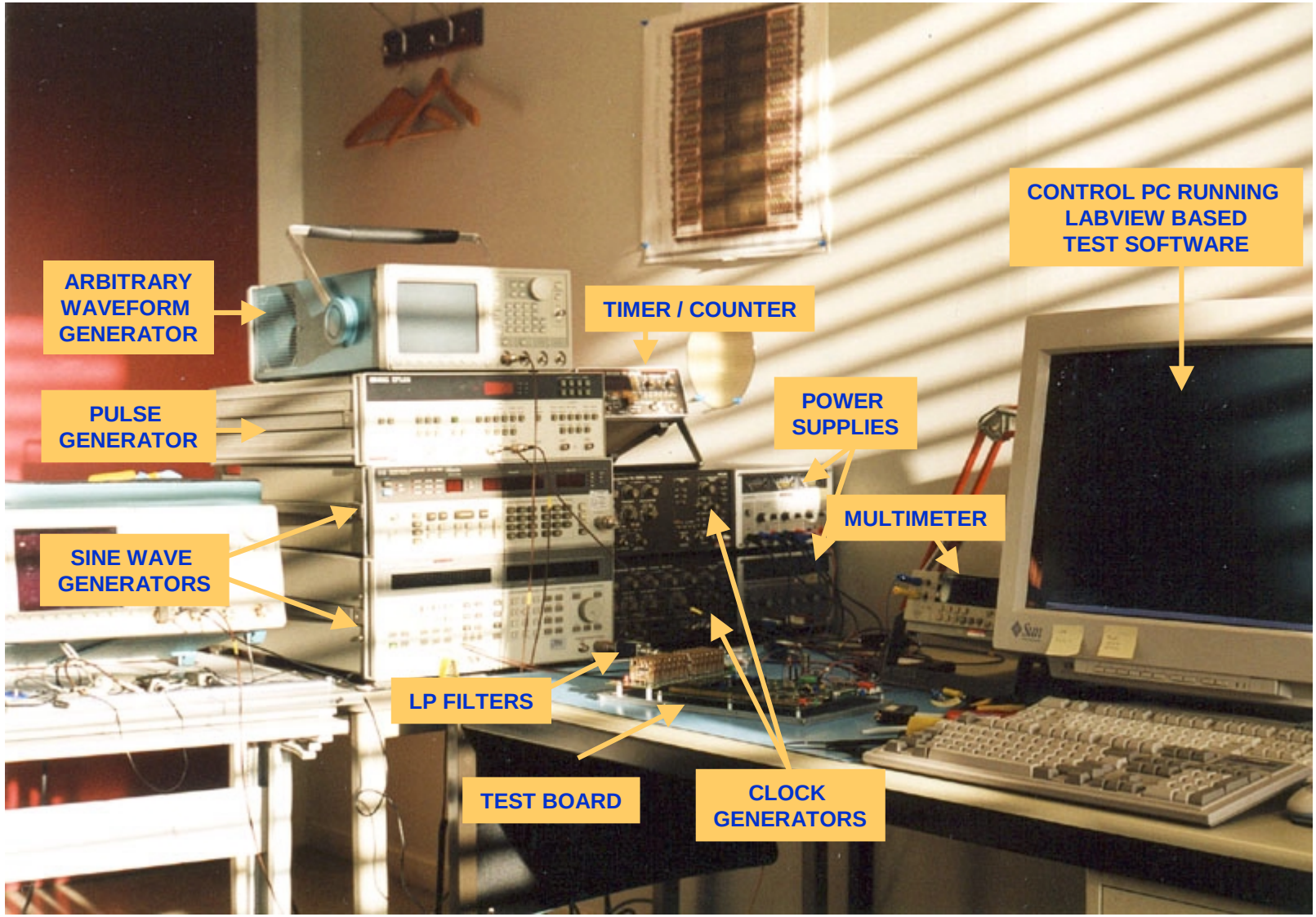
MAX READOUT CLOCK 60 MHz

16-ch signal digitizer and processor

- HCMOS7 0.25 μm (ST)
- area: 64 mm^2
- power: < 20 mW / ch
- prototype delivery: Feb ‘02
- 300 samples fully tested



ALTRO Test Setup



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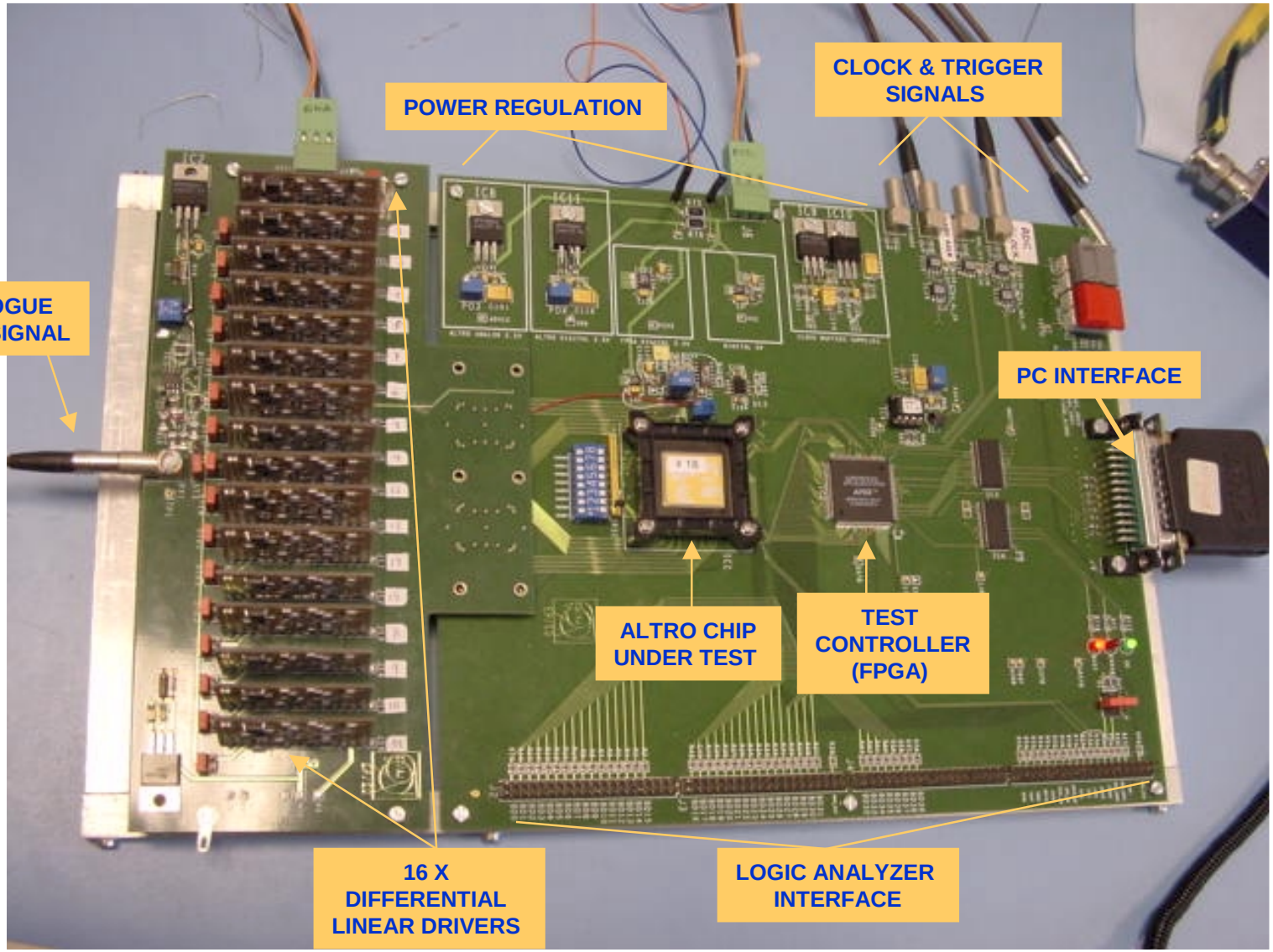
ALTRO Test Board



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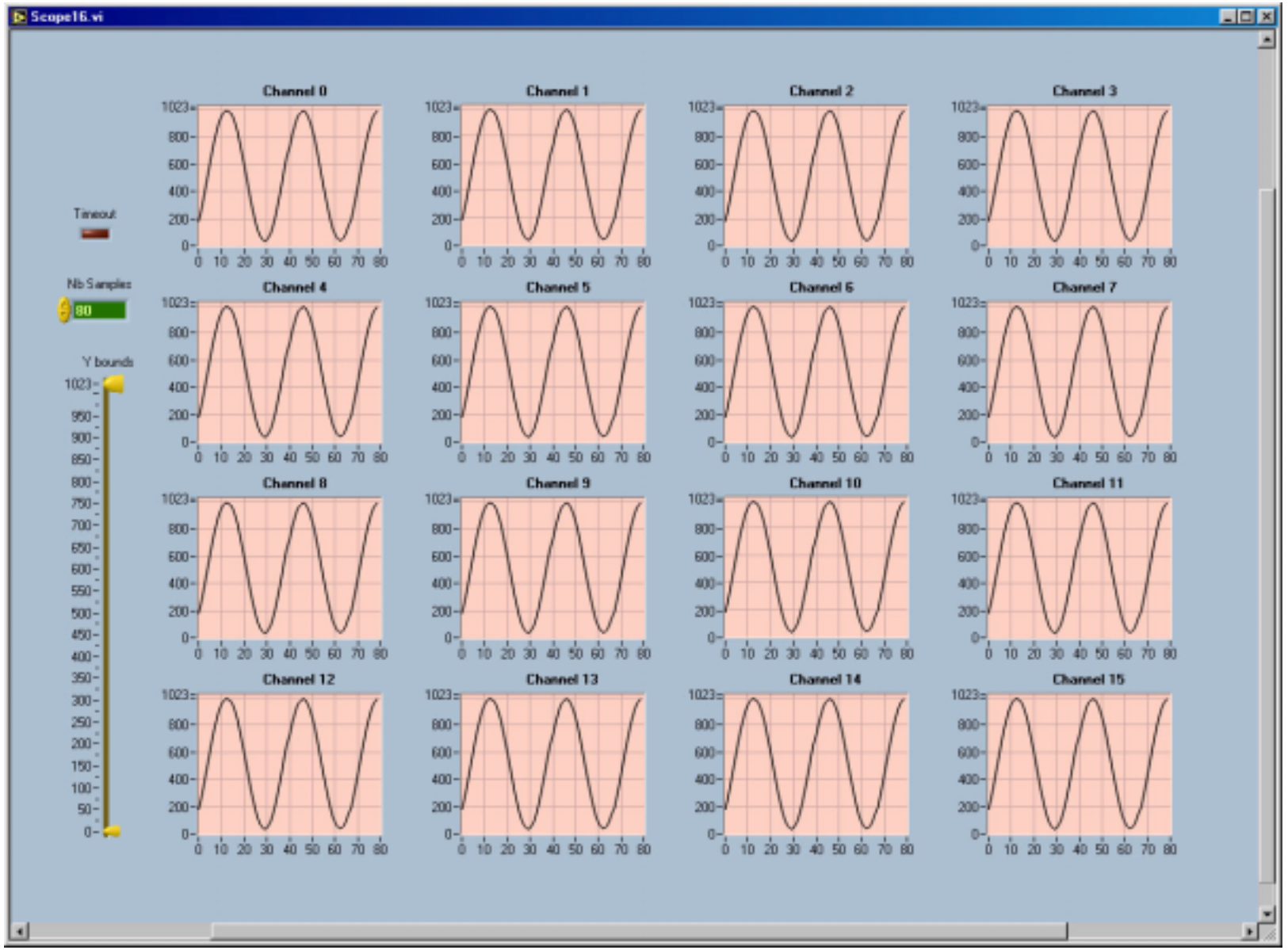
16 channels in one shot



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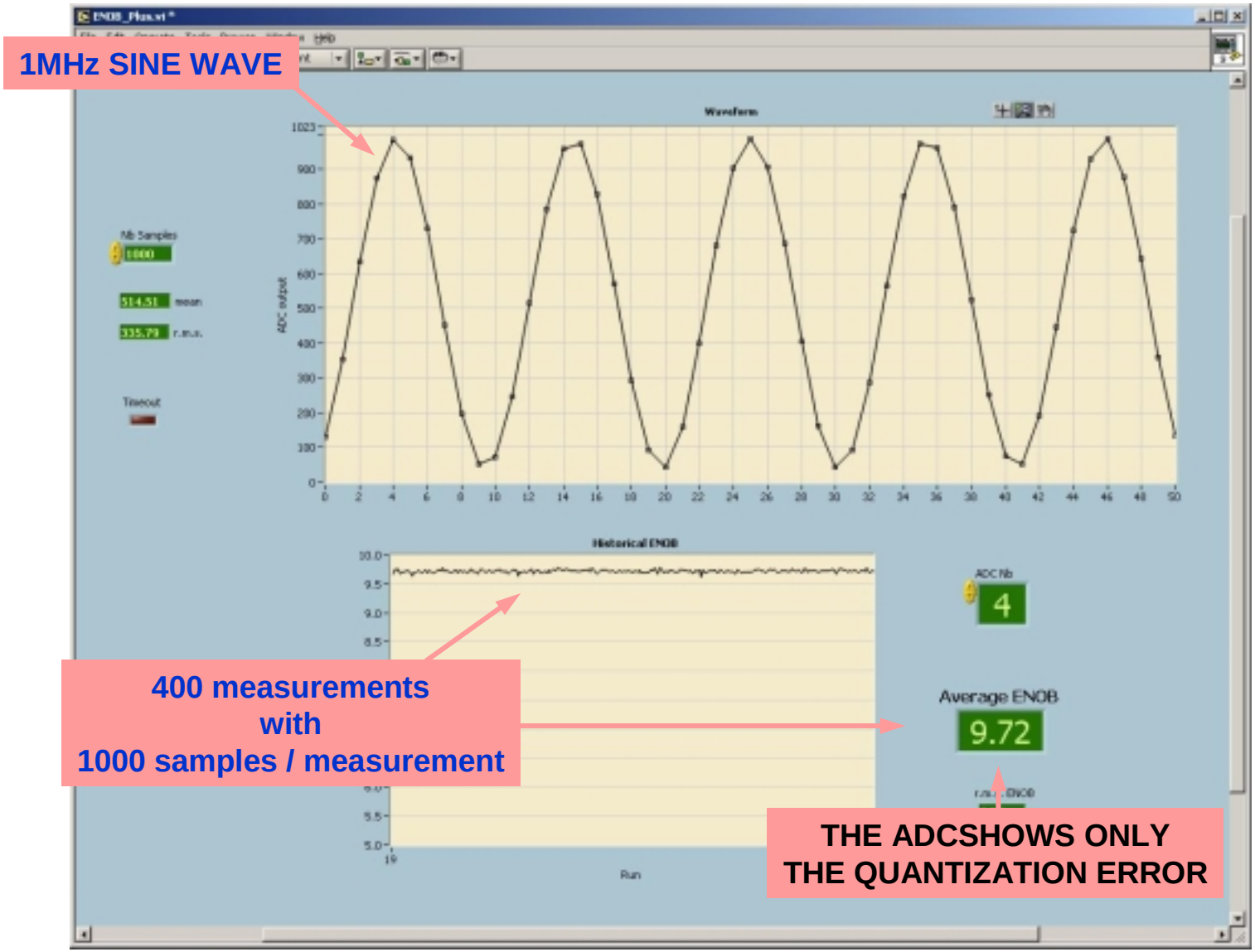
Effective Number of Bits (ENOB)



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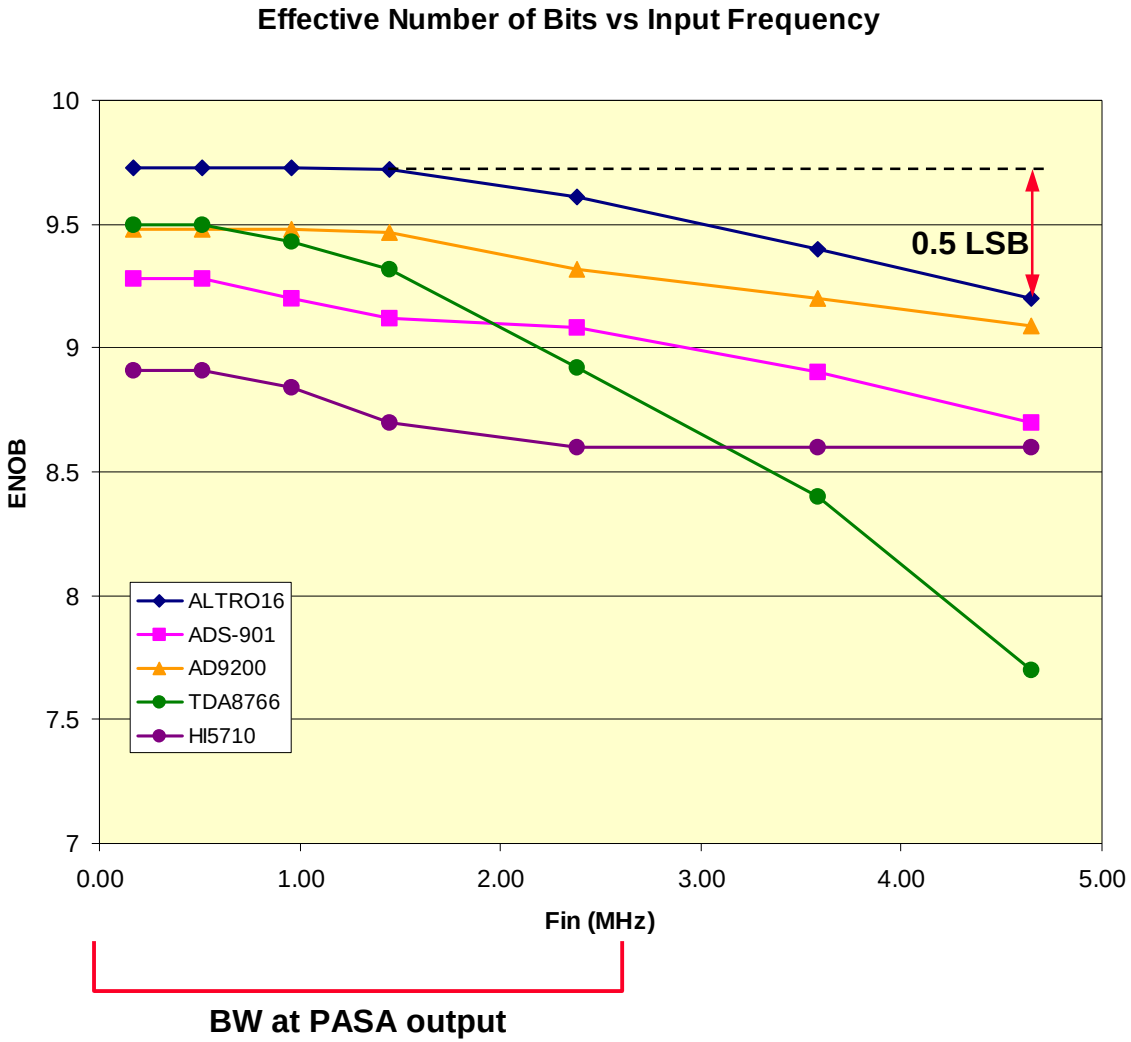
ENOB vs Frequency



Quartz Jitter:

25ps r.m.s.

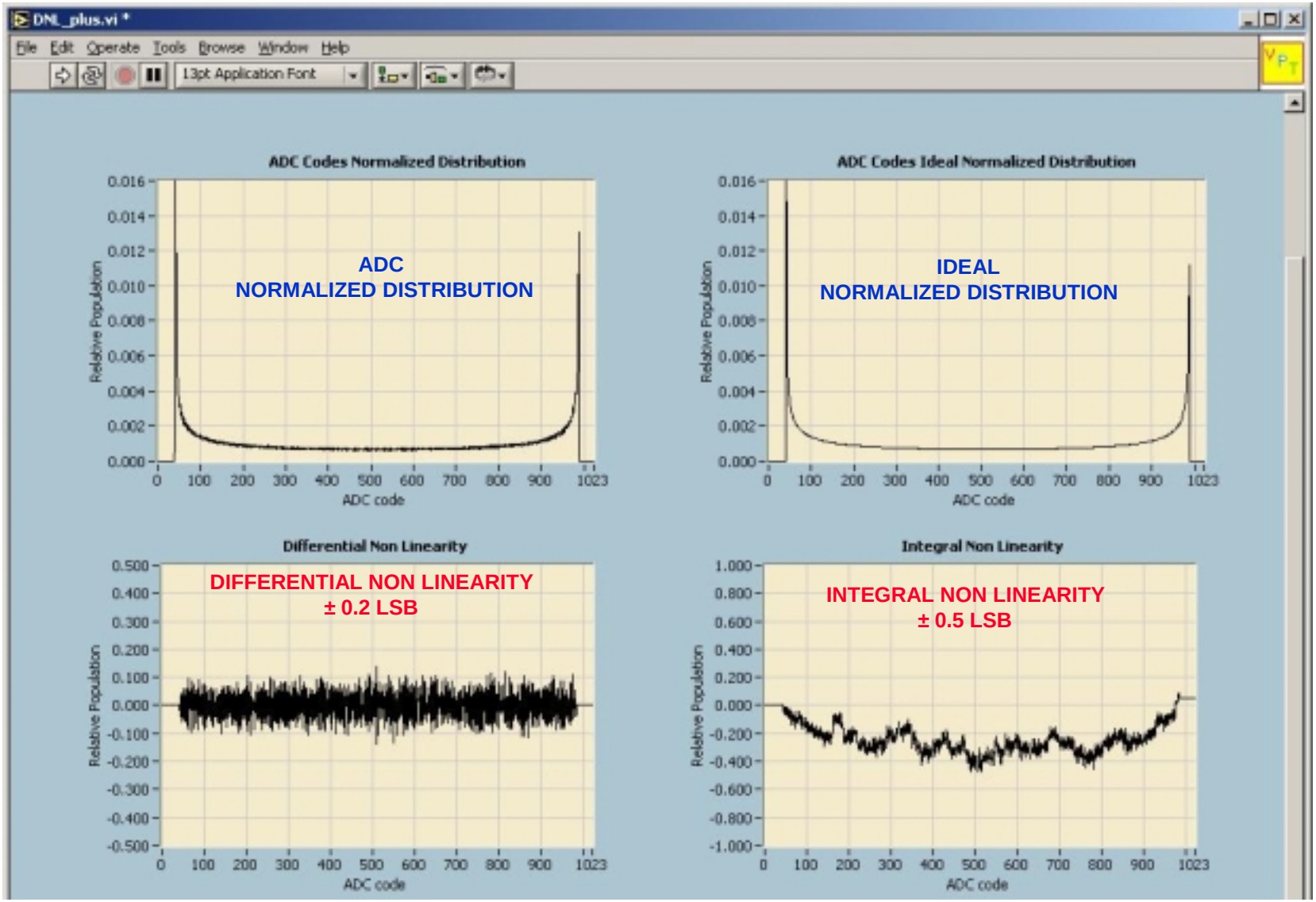
100ps absolute

Amplitude Uncertainty:

$$\frac{\text{jitter}}{4 \cdot f_{in}} \cdot 2^{10}$$

0.5 bits at 4.8 MHz

Differential and Integral Non-Linearity



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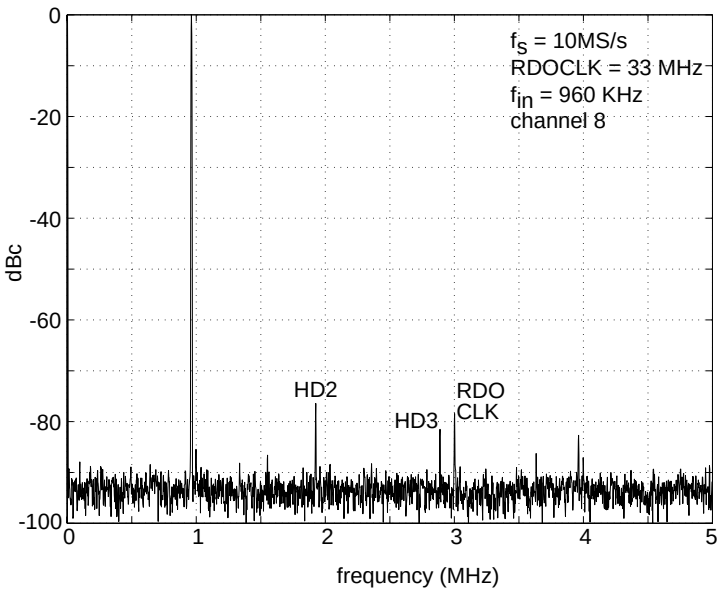
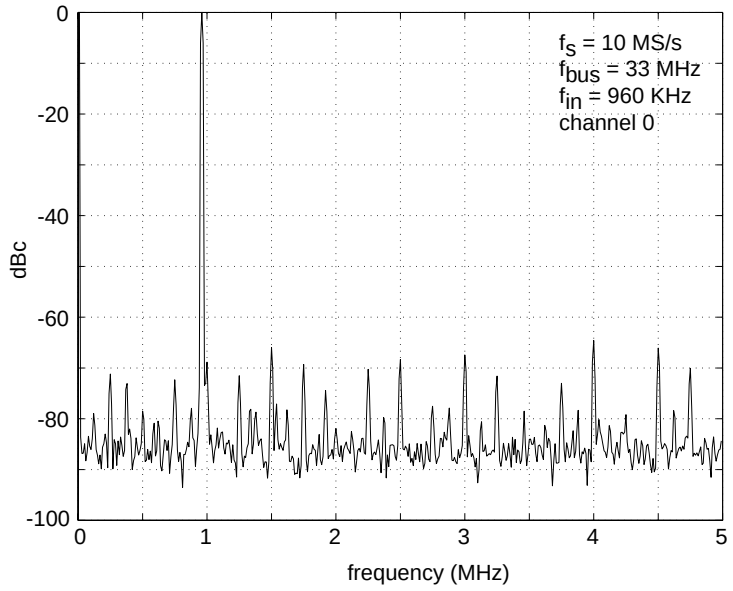
Crosstalk and Digital Noise

DIGITAL NOISE



Readout Clock below -78 dBc (WC)



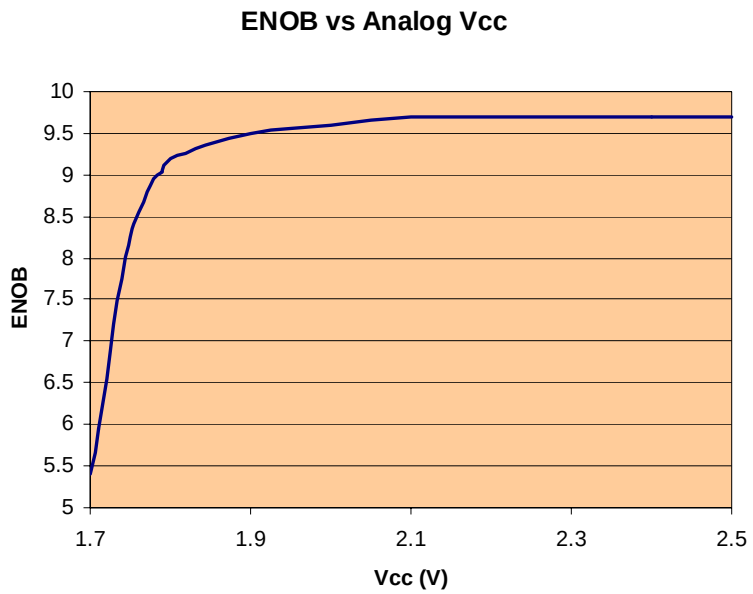
Bus interference below -65 dBc (WC)

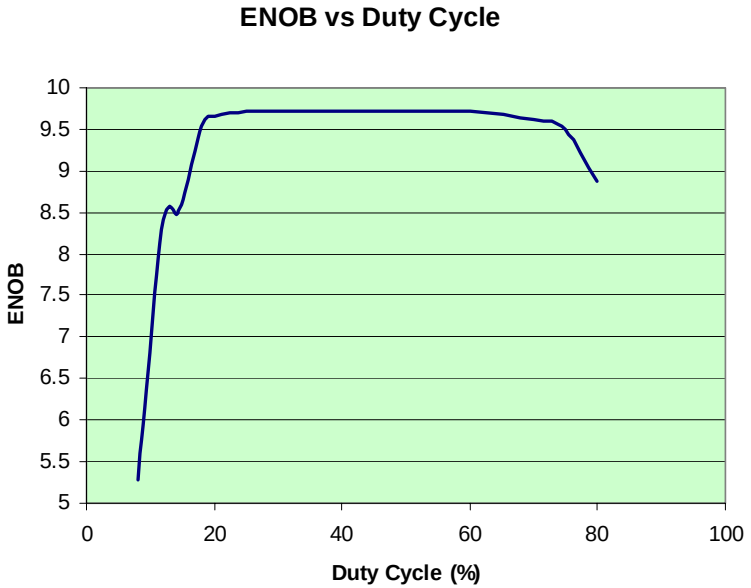
CHANNEL-TO-CHANNEL CROSSTALK

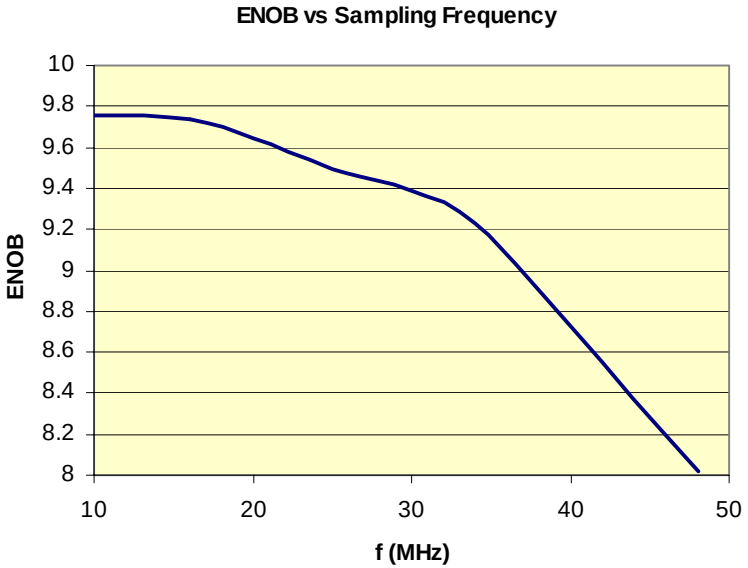
F_{in} = 1 MHz 0.05 LSB rms (-80 dBc)
F_{in} = 5 MHz 0.2 LSB rms (-68 dBc)

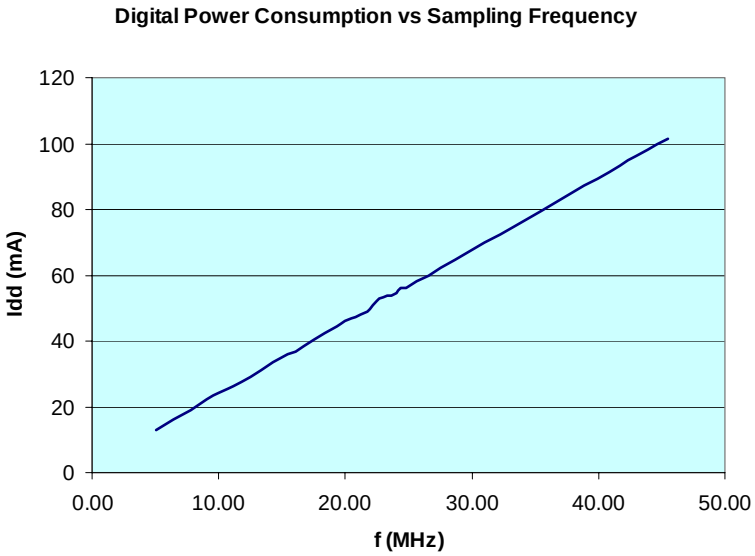
Dynamic Range of a 10-bit ADC: 60 dB

Chip Performance

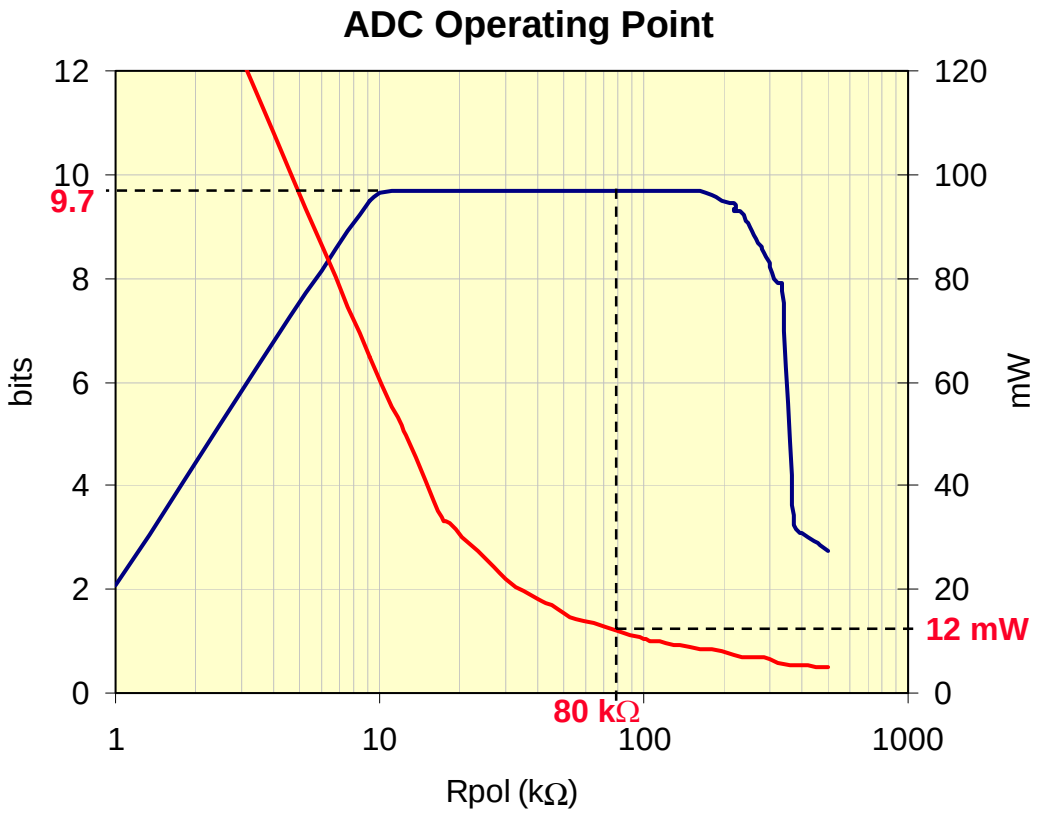








Power Consumption



Effective Number of Bits

Power Consumption per Channel

ONE CHIP		
	Digital leakage current	1.2 mA
	ADC Clock Tree (10 MHz)	23 mA
	Readout Clock Tree (40 MHz)	1.4 mA
	Processing Logic during Trigger (1%)	28 mA
	16 ADCs at 10 MS/s	77 mA

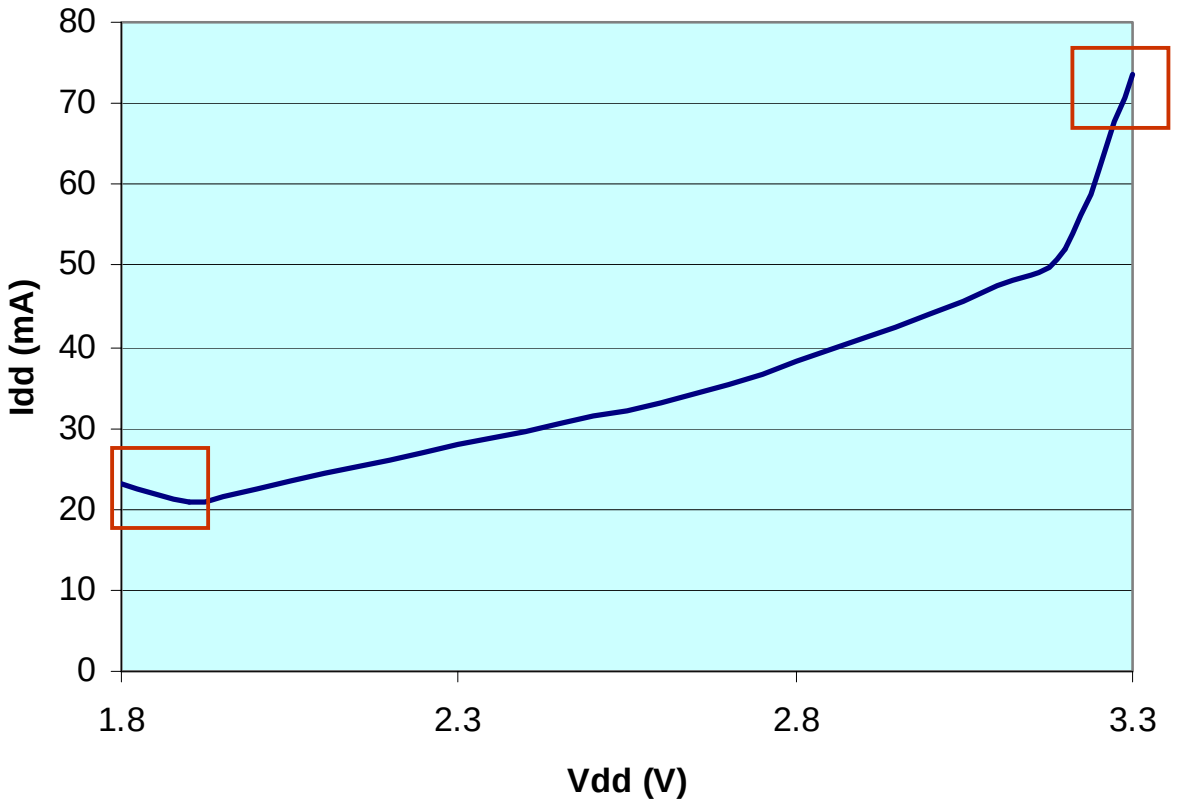
Average Power Per Chip

257 mW

Average Power Per Channel

16 mW

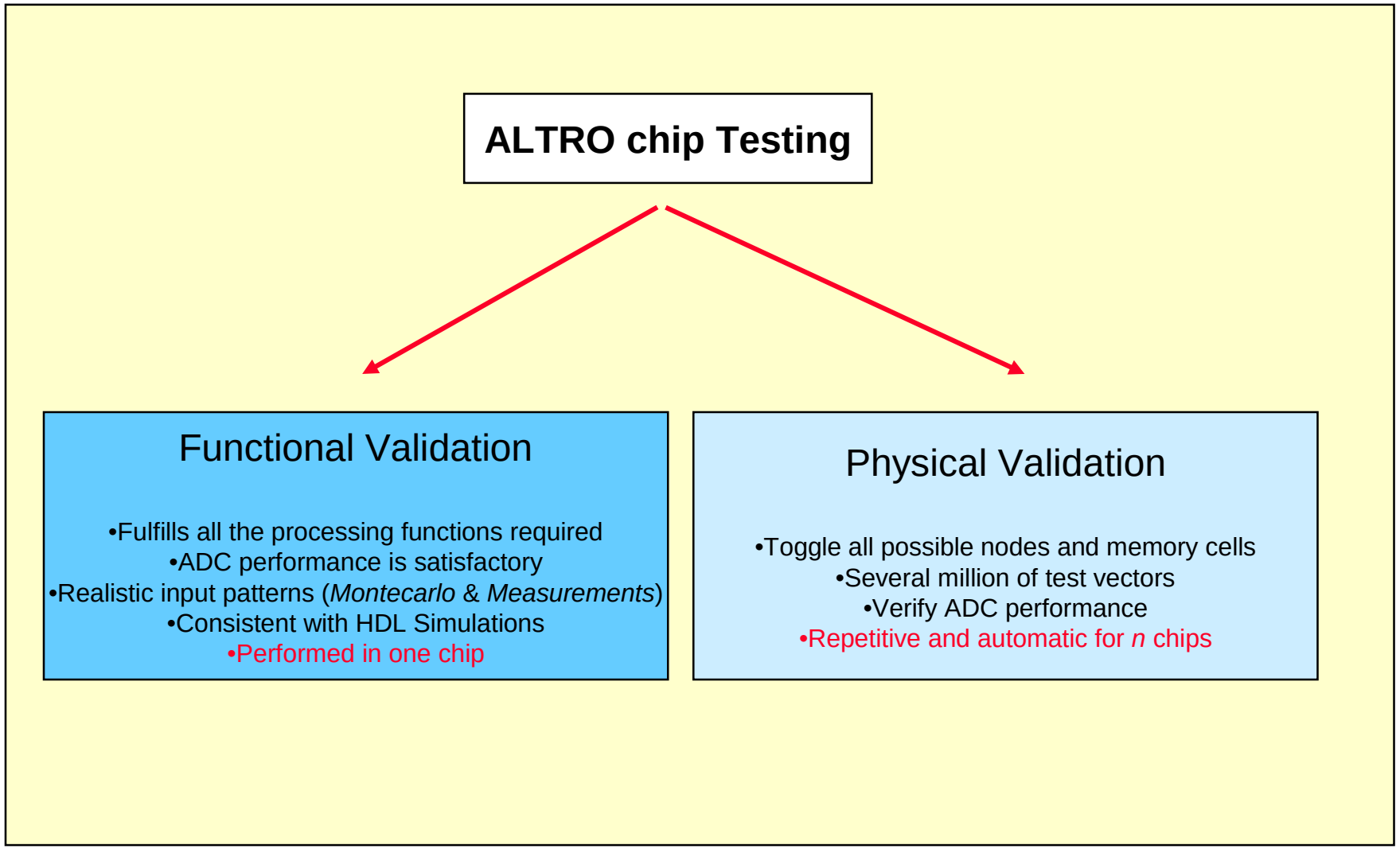
Current vs Digital Supply



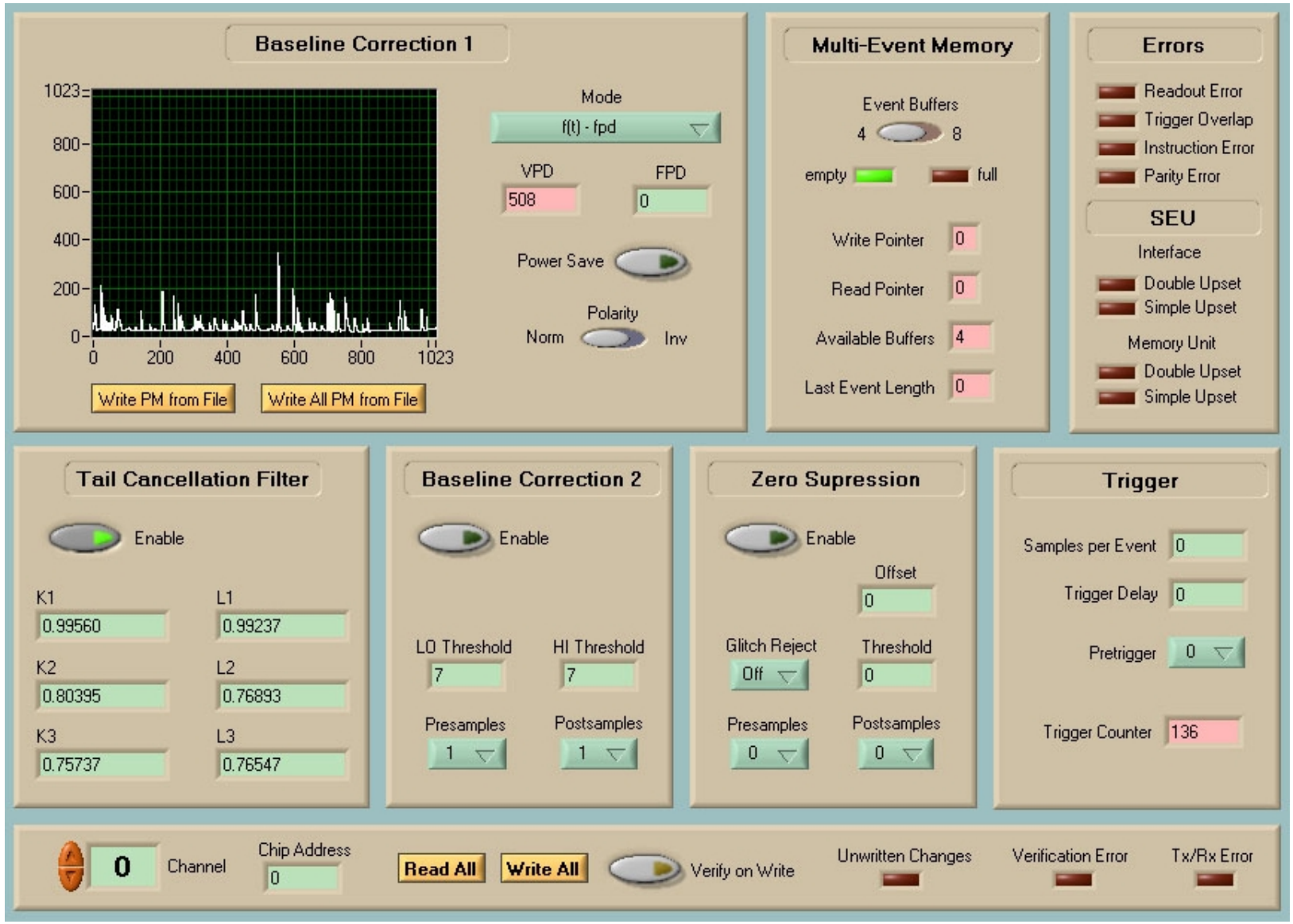
ADC CLK : **10 MHz**
f_{in} : **900 KHz**
I_{pol} : **30 µA (internal resistor)**
V_{cc}: **2.5 V**

ALTRO not responding

Testing Strategy



Functional Validation: Register Control Panel



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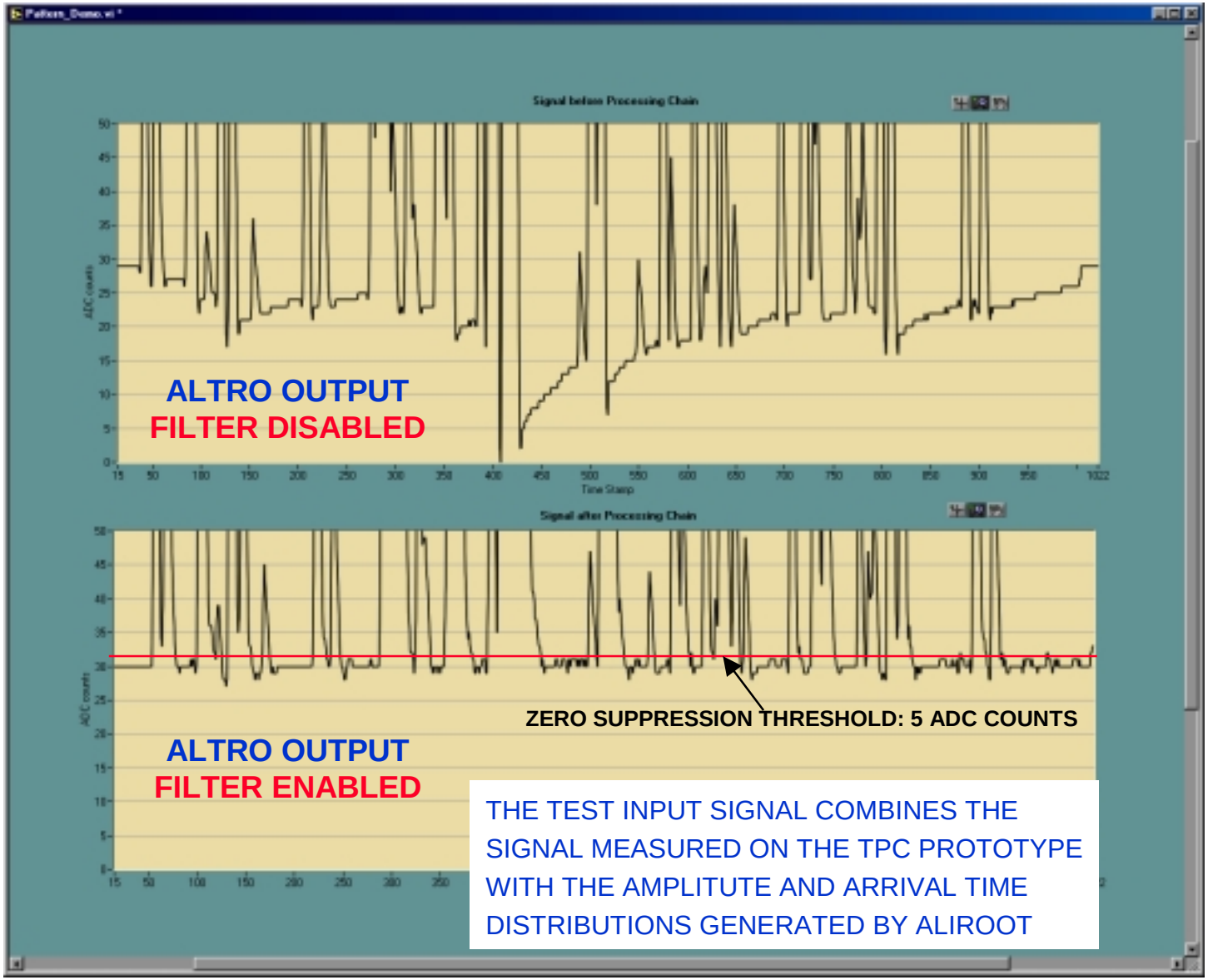
Functional Validation: Realistic Input Pattern



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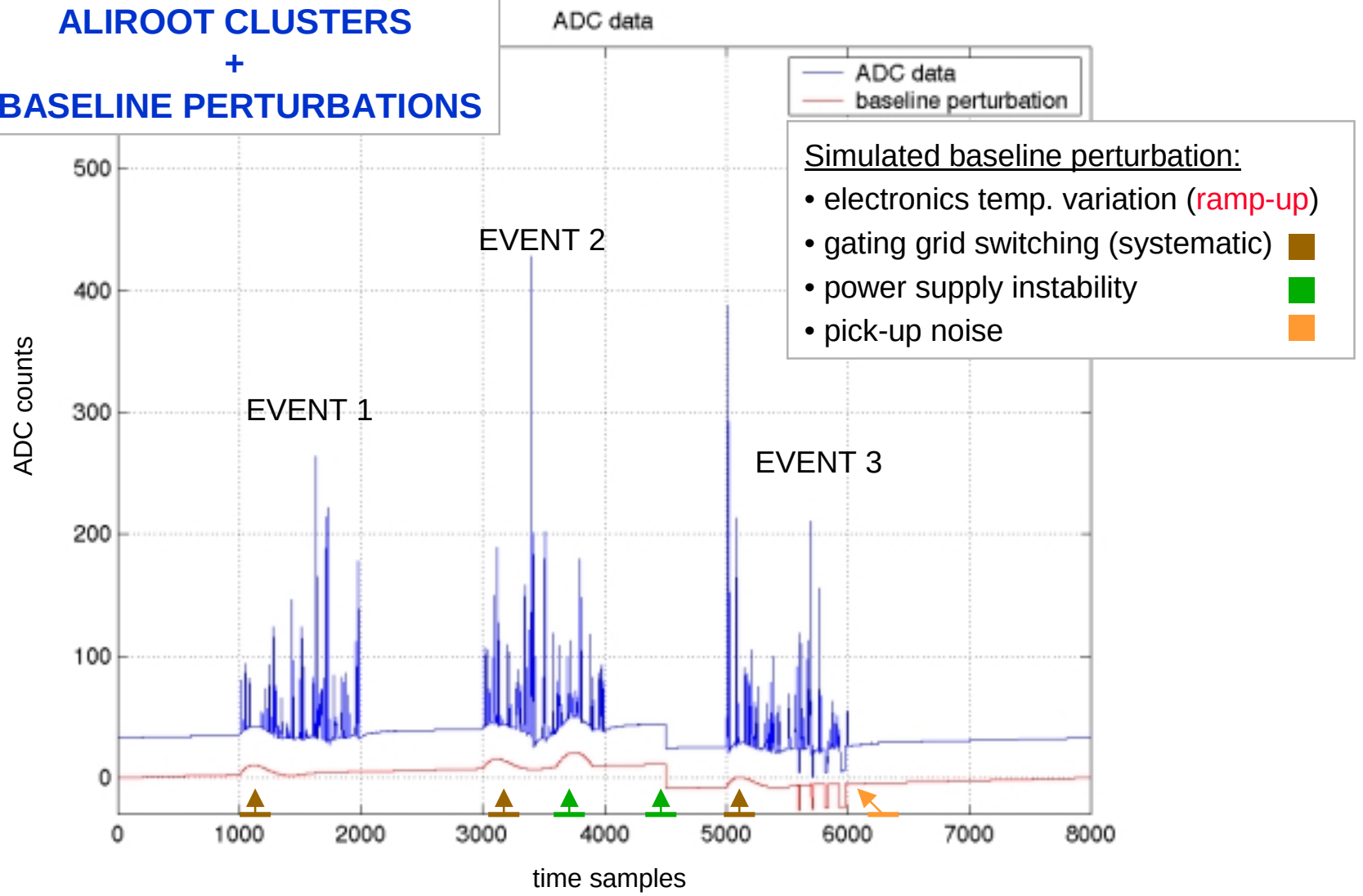
FRONT-END SIGNAL PROCESSING

ALIROOT CLUSTERS
+
BASELINE PERTURBATIONS



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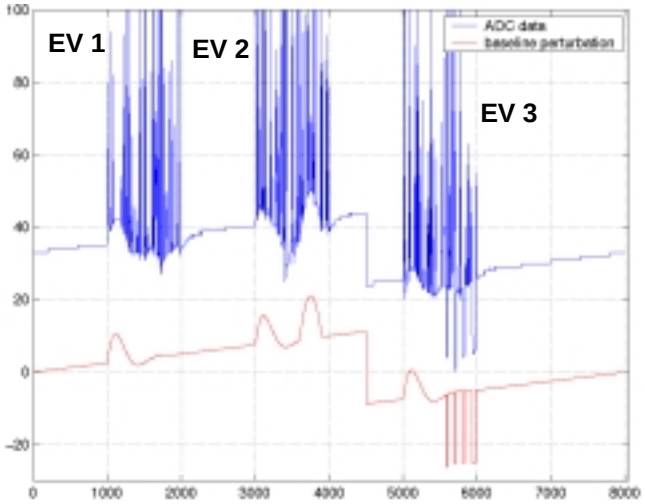
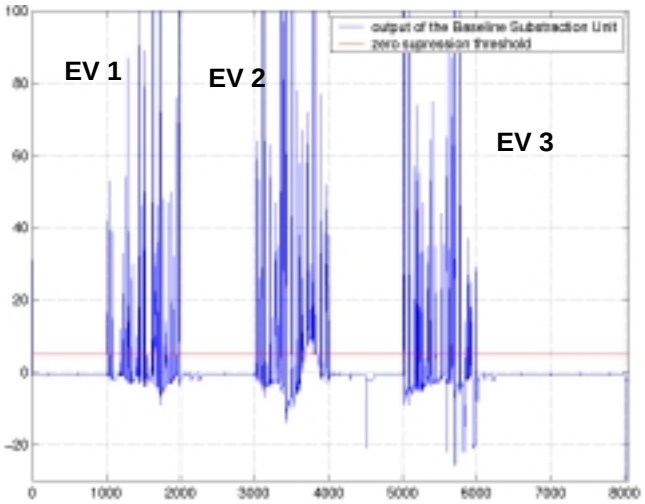
FRONT-END SIGNAL PROCESSING

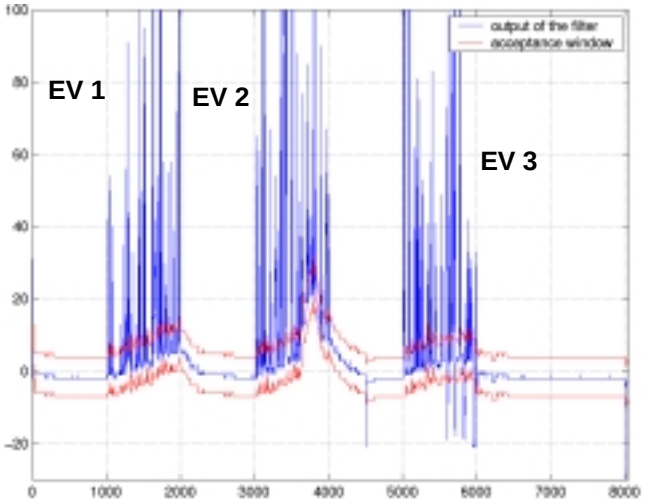
INPUT SIGNAL



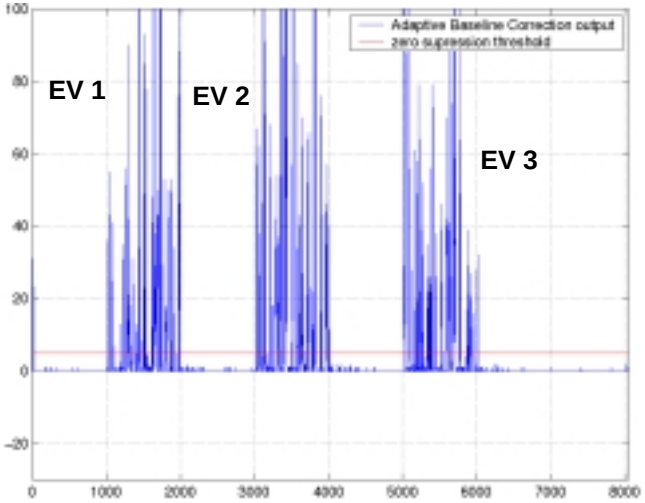
AFTER 1st BASELINE CORRECTION



AFTER TAIL CANCELLATION



AFTER 2nd BASELINE CORRECTION



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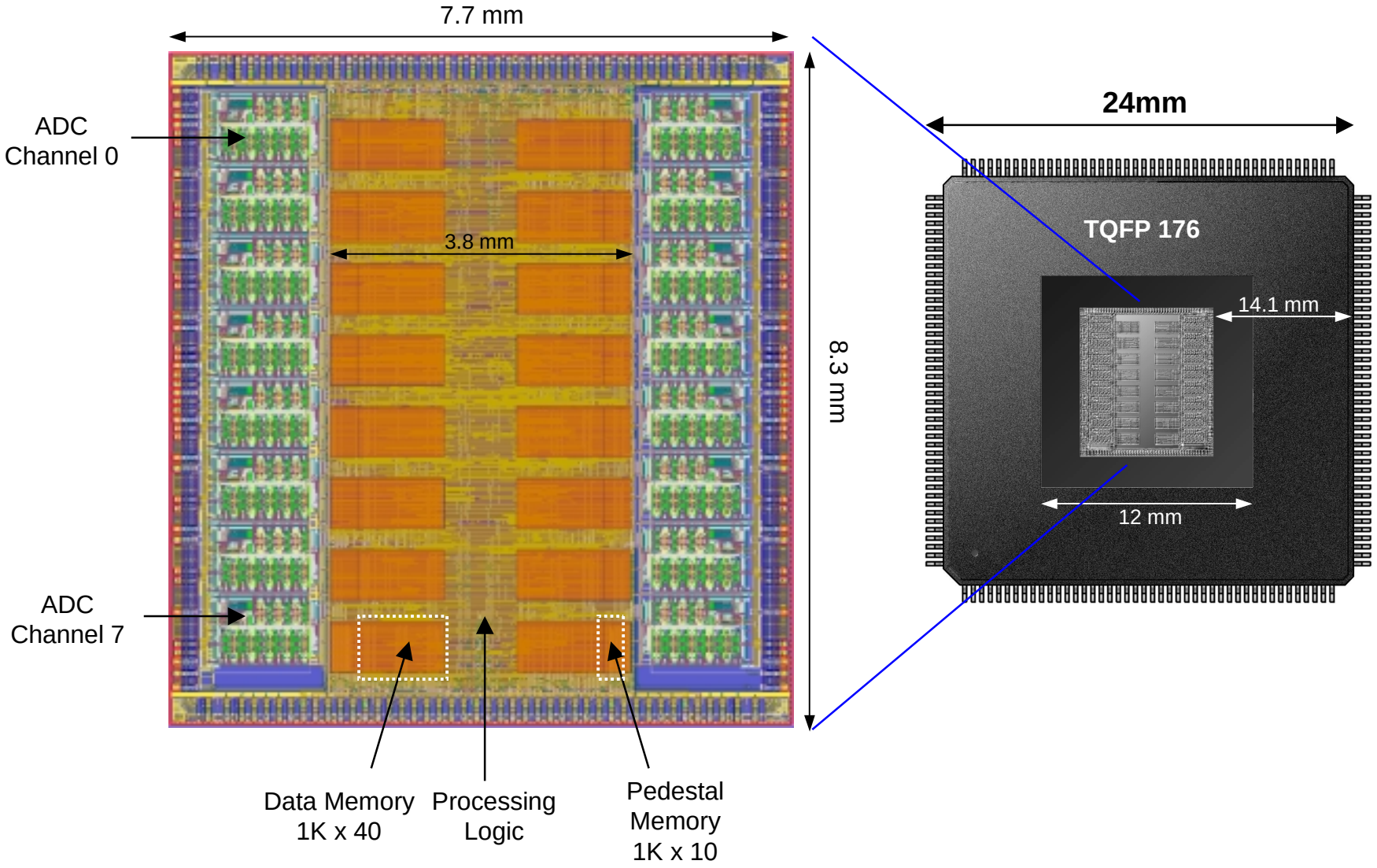
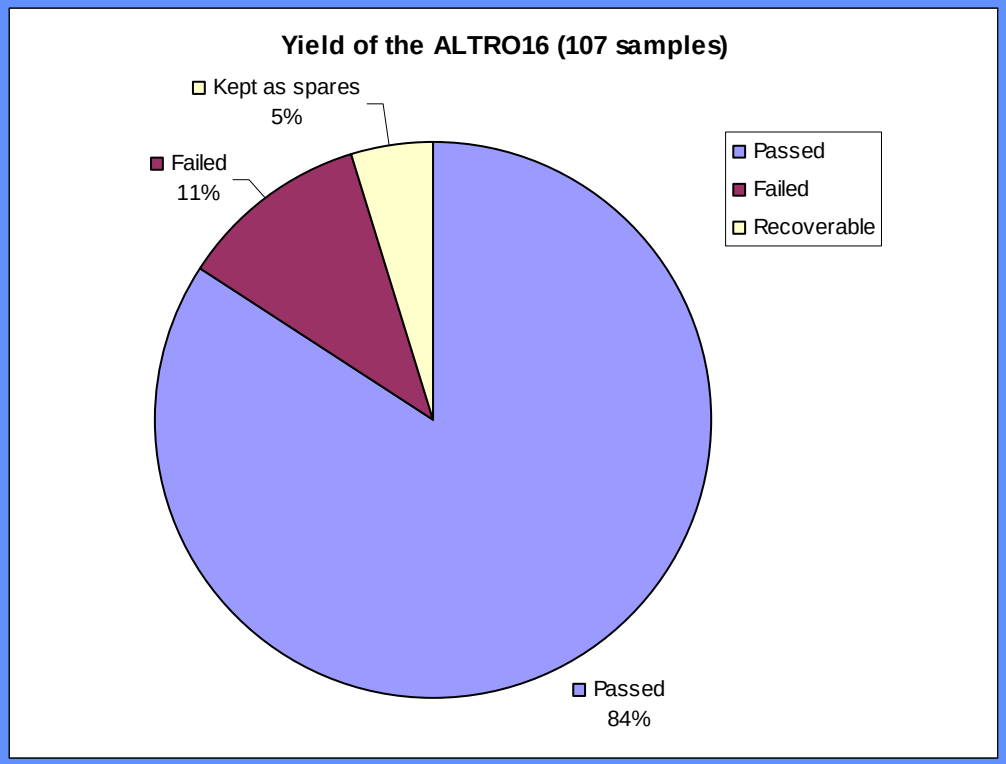
Layout and Package



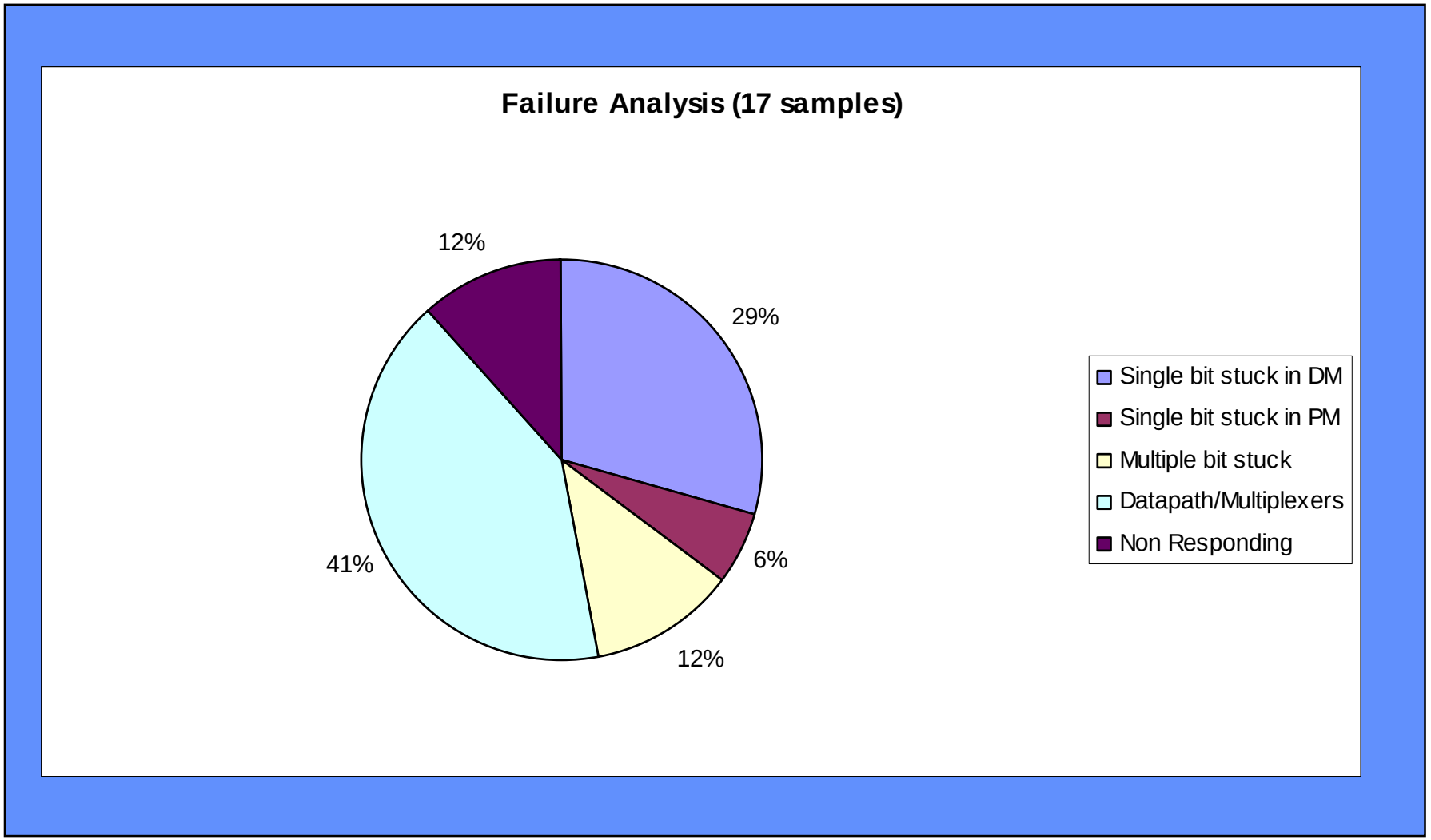
YIELD



Recoverable chips correspond to single and double bit stuck in the Memories

The Specific location of single bit stuck can be known, and the error can be corrected while de-formatting the data packet.

Failure Analysis



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