

ALICE TPC Collaboration Meeting

Hardware and Software for the PASA Bulk Test

Status after the Test of the Engineering Run

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Hard- and Software for the PASA Bulk Test

- Topics
 - Design Objectives
 - Hardware Status
 - Present Test Setup
 - The Test of the Chips of the Engineering Run
 - Planning of the Bulk Test
 - Open Design Issues
 - Some Results of the Test

Hard- and Software for the PASA Bulk Test

- Design Objectives

- Test 50000 Chips @ 80 %Yield in a short time

- 1 Minute Test Time per Chip at 8 hours/day and 5Days/week results in 20 weeks of test time!

- Noise and Speed are Issues

- 30 Mips is only about 150 femto Coulomb

- 220 ns Target Shaping Time needs fast sampling

- Use “well-known” elements of the TPC

- 12 bit ADC from the ST family versus 10 bit in Altro chip

- RCU Card/FEE Bus for connection to PC

Hard- and Software for the PASA Bulk Test

- Hardware

- Features

- 16 independent 14-bit DAC/ 12-bit ADC Channels with local memory on pluggable cards, running at 40 MHz
 - Set PASA voltages (Supply and 3 Reference Voltages) with slow 12-bit DACs
 - Slow 12-bit ADCs for these actual voltages, the connected currents and the static output voltage at 32 pin
 - Pluggable Test socket with Receptacle (only 5000 to 10000 insertions for socket guaranteed)
 - Negative Pulses (inadvertently generated) require 400 us relax time. Handled by hardware.

Hard- and Software for the PASA Bulk Test

- Hardware (cont.)
 - Status
 - One setup fully equipped and tested
 - Another setup manufactured and boards loaded, but needs to be tested
 - Engineering setup with 4/4 channels and similar capabilities is still available when test setup out of house for bulk test
 - Calibration
 - DAC boards generate current. Steps in DAC current generate voltage steps in load resistors on Test Socket Plugin. Coupling Capacitor between these load resistors and PASA input deliver a charge as wanted input stimulus
 - Needed 1 pF coupling capacitors not available better than +/-0.1 pF (+/- 10%). No reference available.

Hard- and Software for the PASA Bulk Test

- Hardware (cont.)
 - Calibration (cont.)
 - DAC Board Full scale current (20 mA) adjusted to better than 1000 ppm and fully interchangeable
 - Input stimulus measured with spectroscopic amplifier at PASA input (without the actual PASA chip) at full scale chip
 - Adjusted to better than 1 % channel to channel match and 250 fC full range on socket plugin
 - Absolute values expected to be in 2.5 % range for statistical reason.

Hard- and Software for the PASA Bulk Test

- Present Test Setup
 - Set up voltages, measure currents and channel output voltages (32 for 16 differential channels)
 - Acquire 32 kiWord samples for each channel with no input stimulus for Noise test
 - With given ADC board local memory size, 512 test windows are dedicated for each channel.
 - Each test window is 400 us long to satisfy the needed negative charge relax time
 - Change DAC to generate useful charge
 - Recorded 32 ADC samples
 - Reset DAC (eventually generating a negative pulse) and discard rest of samples

Hard- and Software for the PASA Bulk Test

- Present Test Setup
 - Test stimulus for each channel
 - 400 pulses forming a linear ramp up to 100fC
 - 52 pulses up to 250 fC
 - 40 pulses forming ramp down to – 250 fC
 - 10 pulses with channel under test with no input, but both neighbours at full scale
 - 10 pulses with channel under test with no input, but all other channels at full scale

Hard- and Software for the PASA Bulk Test

- Present Test Setup
 - Chip parameter calculated from this acquired data
 - Arithmetic and RMS mean of the 32 kiWord Noise sample
 - Gamma 4 fit of the linear ramp up to 70 fC
 - Arithmetic mean of the Gamma 4 fitting parameters (Gain, Offset, peaking Time)
 - Data of all chips at 3.3, 3.0 and 3.6 Volt was written as ASCII file (about 20 MiByte each file, 30 GiByte for 480 Chips at 3 Voltages)
 - Format documented and parsable by e.g. Gnuplot

Hard- and Software for the PASA Bulk Test

- Present Test Setup
 - Screening limits
 - Gain 12mV / fC \pm 20%
 - FWHM = 190ns \pm 20%
 - Current \leq 80mA
- The Test of the Chips of the Engineering Run
 - Socket capacity limits slew rate
 - Pulses over 70 fC not useful to evaluate

Hard- and Software for the PASA Bulk Test

- The Test of the Chips of the Engineering Run
 - Testing Time (per Chip and Voltage Level) for Athlon 2400+ and local disk
 - 4 Second testing time ($16 * 512 * 400$ us)
 - 1 Second Transfer time (to RCU/ to User Memory)
 - 6 Seconds for Calculations, mostly about 5000 Gamma 4 Fits (using GSL Library)
 - With handling and manual marking total 1 Minute by skilled worker
 - RCU/FEE observation
 - Better mechanical connection between mezzanine/ board
 - FEE connectors on mezzanine should have clamps

Hard- and Software for the PASA Bulk Test

- The Test of the Chips of the Engineering Run
 - Most failing chips showed excessive supply current
 - 53 chips of 480 tested chips failed (89 % yield).
Closer inspection of failing Chips perhaps usefull.
 - Dust sometimes caused Half/No Gain indication.
Visual inspection an reinsertion needed for that case
 - PASA Chip in Socket more noise sensitive than soldered directly to board. Shielding used, so additional steps for each ship needed
 - Test at Min/Max voltage didn't show up new defects

Hard- and Software for the PASA Bulk Test

- Plans for the Bulk Test
 - Agreement with Lund to use the Robot at Lund
 - Hired external workforce on PASA testing budget
 - PASA Test setup with dedicated PC delivered to Lund. Communication between Robot and Tester Socket based (probably Ethernet)
 - Agreement on exact test agenda
 - Full Test for Min/Max voltage needed?
 - Classification?
 - Sacrifice statistics for testing speed

Hard- and Software for the PASA Bulk Test

- Open Design Issues
 - Clamp Shell/ Open Top Socket?
 - Clamp Shell socket used for ALTRO test
 - Open Top Socket needs clamping mechanism, but allows Robot to serve second test setup interleaved and eventually a shield
 - Capacitive load seems same
 - Keep lead time 8-12 weeks in mind. Have enough spares
 - Air flow into socket/ over Chip to remove dust?